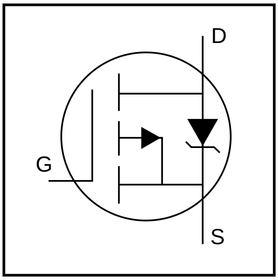
International
IOR Rectifier

PD - 9.1485B

IRF9Z34N

HEXFET® Power MOSFET

- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- P-Channel
- Fully Avalanche Rated



V_{DSS} = -55V

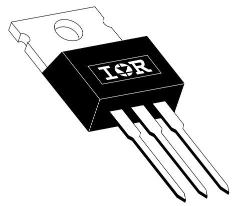
$R_{DS(on)}$ = 0.10Ω

I_D = -19A

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.



TO-220AB

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ -10V	-19	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ -10V	-14	
I_{DM}	Pulsed Drain Current ①	-68	
P_D @T_C = 25°C	Power Dissipation	68	W
	Linear Derating Factor	0.45	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②	180	mJ
I_{AR}	Avalanche Current①	-10	A
E_{AR}	Repetitive Avalanche Energy①	6.8	mJ
dv/dt	Peak Diode Recovery dv/dt ③	-5.0	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	2.2	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	62	

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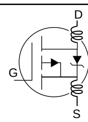
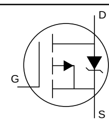
Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-55	–––	–––	V	V_{GS} = 0V, I_D = -250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	–––	-0.05	–––	V/°C	Reference to 25°C, I_D = -1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	–––	–––	0.10	Ω	V_{GS} = -10V, I_D = -10A ④
$V_{GS(th)}$	Gate Threshold Voltage	-2.0	–––	-4.0	V	V_{DS} = V_{GS}, I_D = -250μA
g_{fs}	Forward Transconductance	4.2	–––	–––	S	V_{DS} = 25V, I_D = -10A
I_{DSS}	Drain-to-Source Leakage Current	–––	–––	-25	μA	V_{DS} = -55V, V_{GS} = 0V
		–––	–––	-250		V_{DS} = -44V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	–––	–––	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	–––	–––	-100		V_{GS} = -20V
Q_g	Total Gate Charge	–––	–––	35	nC	I_D = -10A
Q_{gs}	Gate-to-Source Charge	–––	–––	7.9		V_{DS} = -44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	–––	–––	16		V_{GS} = -10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	–––	13	–––	ns	V_{DD} = -28V
t_r	Rise Time	–––	55	–––		I_D = -10A
$t_{d(off)}$	Turn-Off Delay Time	–––	30	–––		R_G = 13Ω
t_f	Fall Time	–––	41	–––		R_D = 2.6Ω, See Fig. 10 ④
L_D	Internal Drain Inductance	–––	4.5	–––	nH	Between lead, 6mm (0.25in.)
L_S	Internal Source Inductance	–––	7.5	–––		from package and center of die contact 
C_{iss}	Input Capacitance	–––	620	–––	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	–––	280	–––		V_{DS} = -25V
C_{rss}	Reverse Transfer Capacitance	–––	140	–––		f = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	–––	–––	-19	A	MOSFET symbol showing the
I_{SM}	Pulsed Source Current (Body Diode) ①	–––	–––	-68		integral reverse p-n junction diode. 
V_{SD}	Diode Forward Voltage	–––	–––	-1.6	V	T_J = 25°C, I_S = -10A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	–––	54	82	ns	T_J = 25°C, I_F = -10A
Q_{rr}	Reverse RecoveryCharge	–––	110	160	nC	di/dt = -100A/μs ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L_S+L_D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 3.6mH R_G = 25Ω, I_{AS} = -10A. (See Figure 12)

③ $I_{SD} \le$ -10A, di/dt $\le$ -290A/μs, $V_{DD} \le V_{(BR)DSS}$, $T_J \le$ 175°C

④ Pulse width $\le$ 300μs; duty cycle $\le$ 2%.

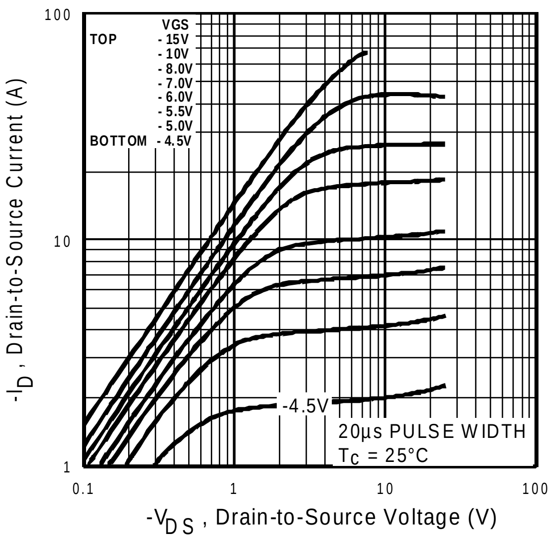


Fig 1. Typical Output Characteristics

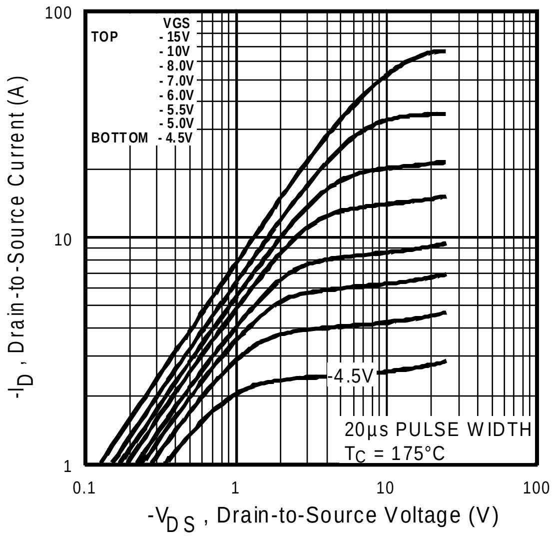


Fig 2. Typical Output Characteristics

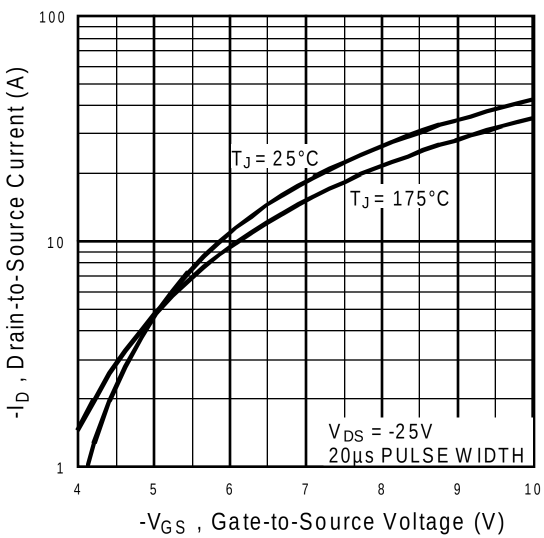


Fig 3. Typical Transfer Characteristics

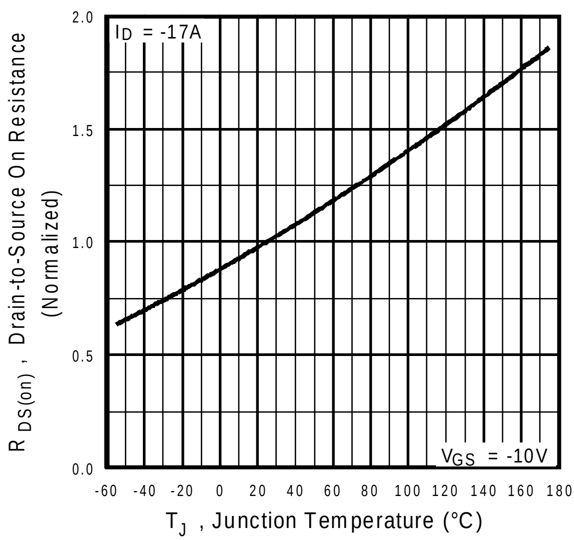


Fig 4. Normalized On-Resistance Vs. Temperature

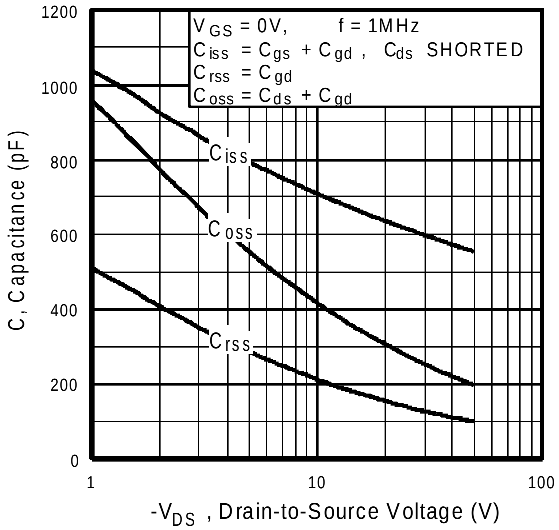


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

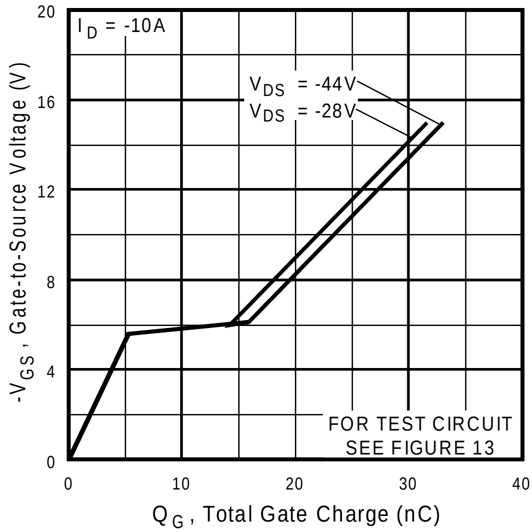


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

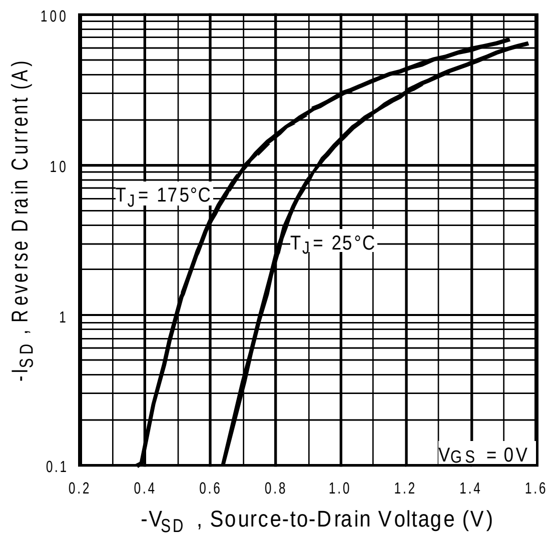


Fig 7. Typical Source-Drain Diode Forward Voltage

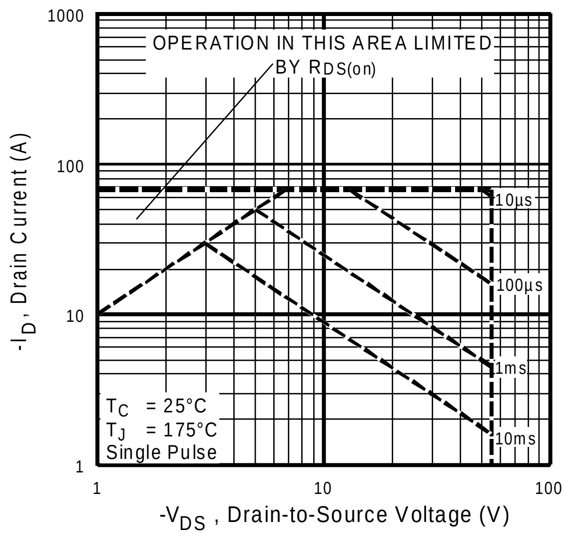


Fig 8. Maximum Safe Operating Area

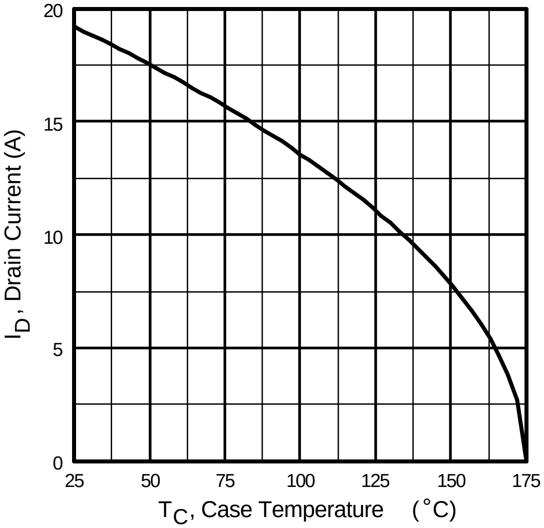


Fig 9. Maximum Drain Current Vs. Case Temperature

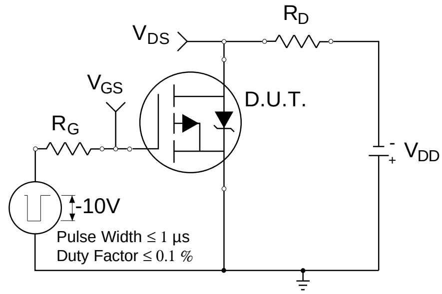


Fig 10a. Switching Time Test Circuit

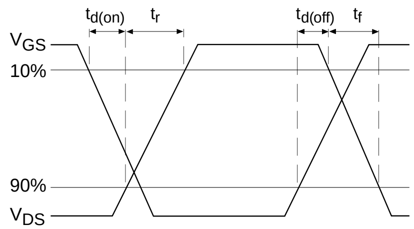


Fig 10b. Switching Time Waveforms

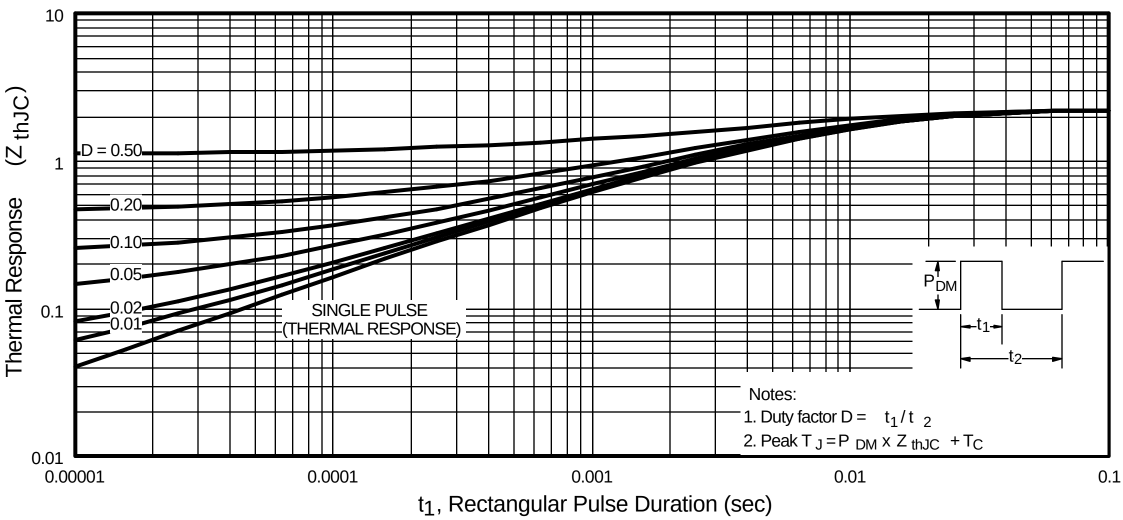


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

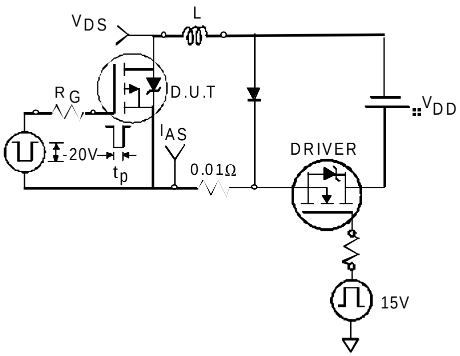


Fig 12a. Unclamped Inductive Test Circuit

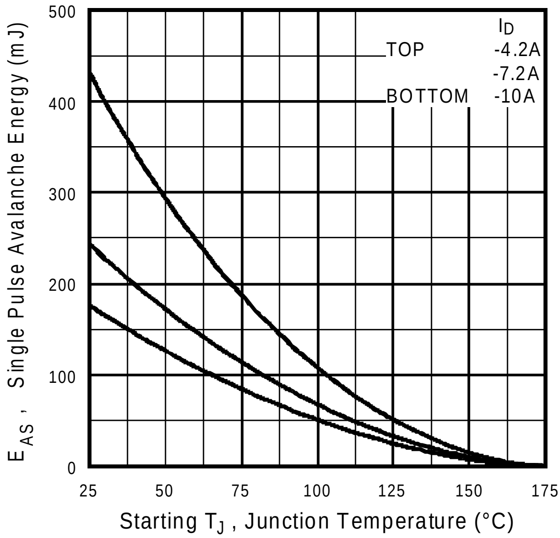


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

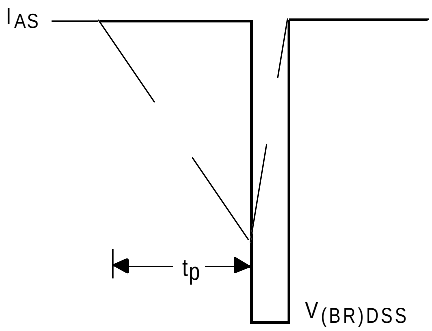


Fig 12b. Unclamped Inductive Waveforms

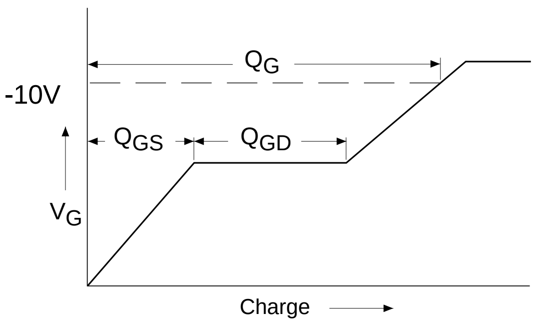


Fig 13a. Basic Gate Charge Waveform

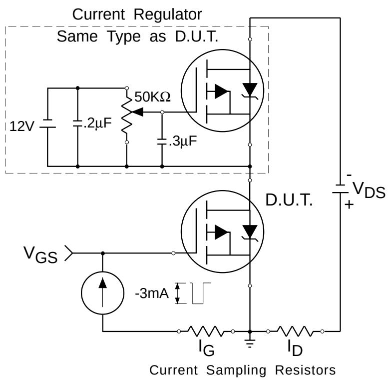
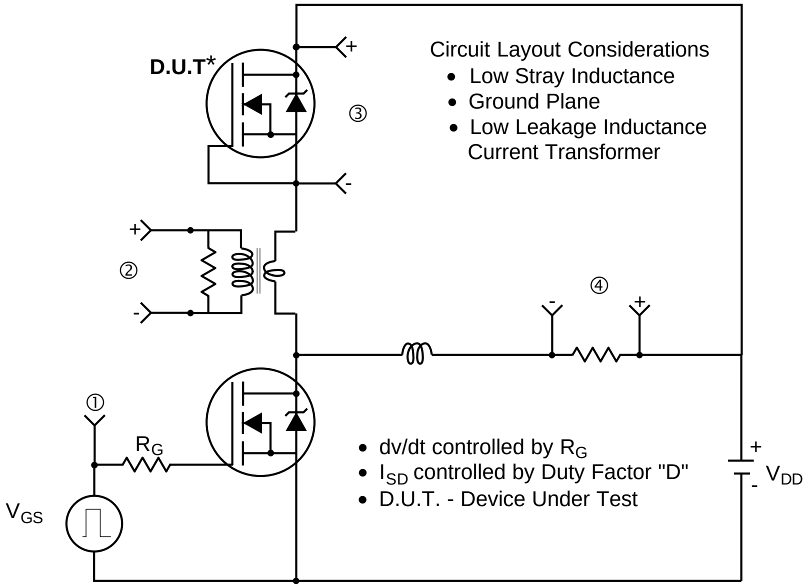
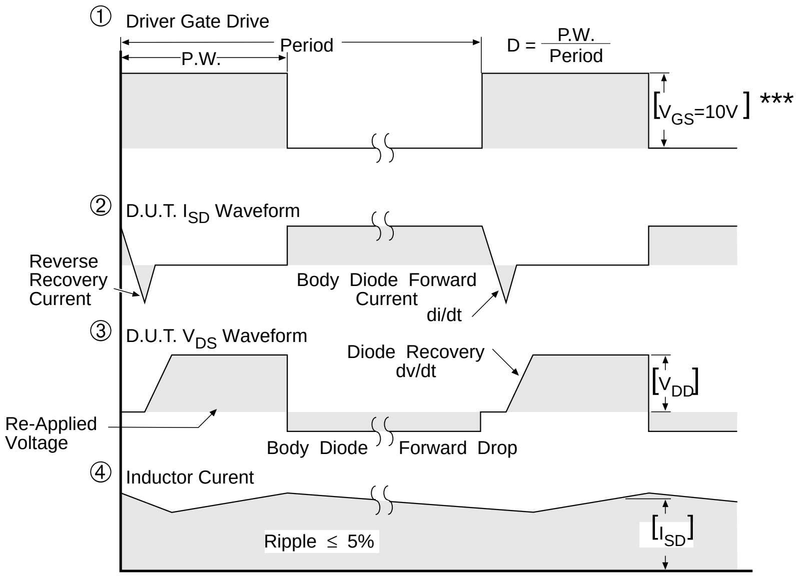


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



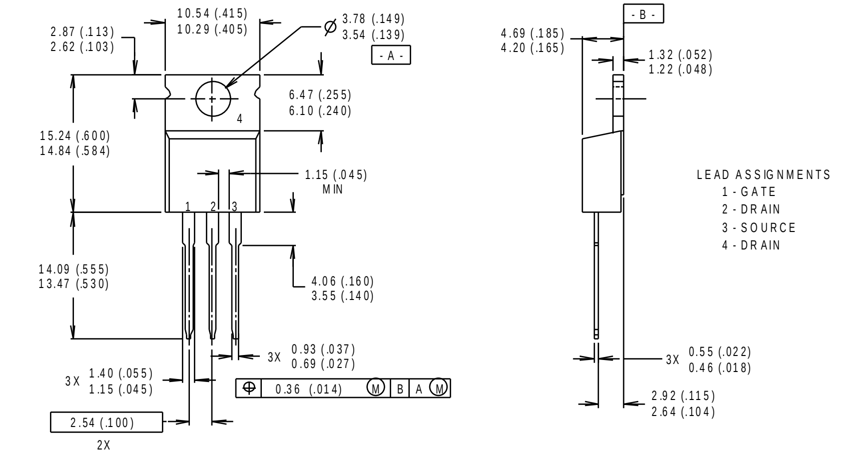
*** V_{GS} = 5.0V for Logic Level and 3V Drive Devices

Fig 14. For P-Channel HEXFETS

Package Outline

TO-220AB Outline

Dimensions are shown in millimeters (inches)



NOTES:

1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.

2 CONTROLLING DIMENSION : INCH

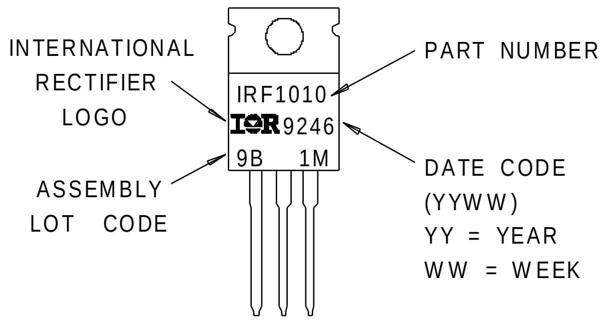
3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.

4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

Part Marking Information

TO-220AB

EXAMPLE : THIS IS AN IRF1010
WITH ASSEMBLY
LOT CODE 9B1M



International
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