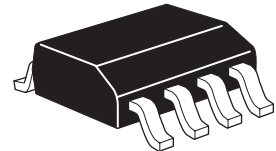


ZXMN6A25DN8

Dual 60V SO8 N-channel enhancement mode MOSFET

Summary

$V_{(BR)DSS}$	$R_{DS(on)}$ (Ω)	I_D (A)
60	0.050 @ $V_{GS} = 10V$	5
	0.070 @ $V_{GS} = 4.5V$	4.2



Description

This new generation trench MOSFET from Zetex features a unique structure combining the benefits of low on-resistance and fast switching, making it ideal for high efficiency power management applications.

Features

- Low on-resistance
- Fast switching speed
- Low gate drive
- Low profile SO8 package

Applications

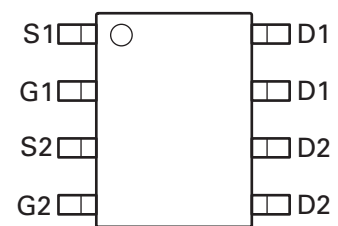
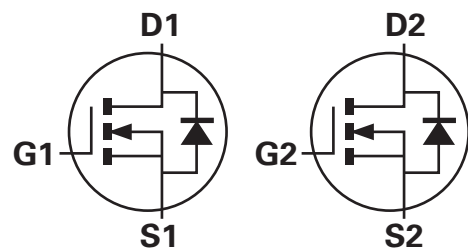
- DC - DC converters
- Power management functions
- Motor control

Ordering information

Device	Reel (inches)	Tape width (mm)	Quantity per reel
ZXMN6A25DN8TA	7	12	500
ZXMN6A25DN8TC	13	12	2500

Device marking

ZXMN
6A25D



Pin out - top view

ZXMN6A25DN8

Absolute maximum ratings

Parameter	Symbol	Limit	Unit
Drain-source voltage	V_{DSS}	60	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current @ $V_{GS}=10V$; $T_{amb}=25^{\circ}C^{(b)}$ (d)	I_D	5	A
@ $V_{GS}=10V$; $T_{amb}=70^{\circ}C^{(b)}$ (d)		4	A
@ $V_{GS}=10V$; $T_{amb}=25^{\circ}C^{(a)}$ (d)		3.8	A
Pulsed drain current ^(c)	I_{DM}	24	A
Continuous source current (body diode) ^(b)	I_S	3.4	A
Pulsed source current (body diode) ^(c)	I_{SM}	24	A
Power dissipation at $T_{amb}=25^{\circ}C^{(a)}$ (d)	P_D	1.25	W
Linear derating factor		10	mW/ $^{\circ}C$
Power dissipation at $T_{amb}=25^{\circ}C^{(a)}$ (e)	P_D	1.8	W
Linear derating factor		14	mW/ $^{\circ}C$
Power dissipation at $T_{amb}=25^{\circ}C^{(b)}$ (d)	P_D	2.1	W
Linear derating factor		17	mW/ $^{\circ}C$
Operating and storage temperature range	$T_j:T_{stg}$	-55 to +150	$^{\circ}C$

Thermal resistance

Parameter	Symbol	Limit	Unit
Junction to ambient ^(a) (d)	$R_{\theta JA}$	100	$^{\circ}C/W$
Junction to ambient ^(a) (e)	$R_{\theta JA}$	70	$^{\circ}C/W$
Junction to ambient ^(b) (d)	$R_{\theta JA}$	60	$^{\circ}C/W$

NOTES:

(a) For a device surface mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions.

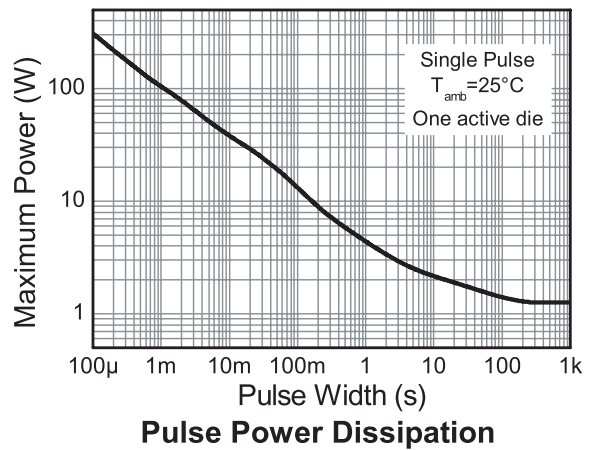
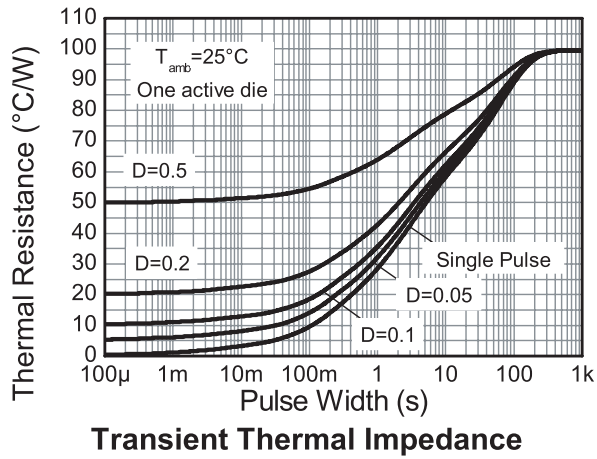
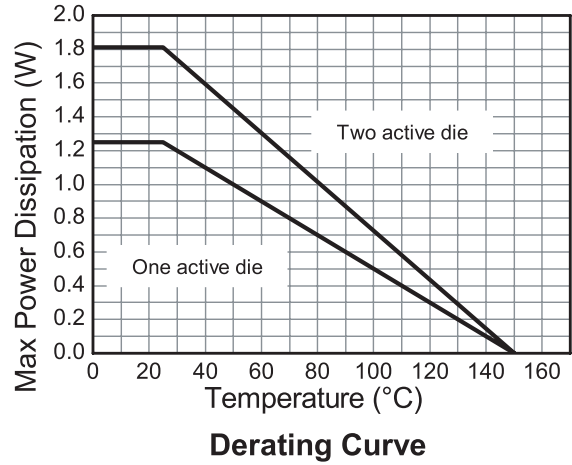
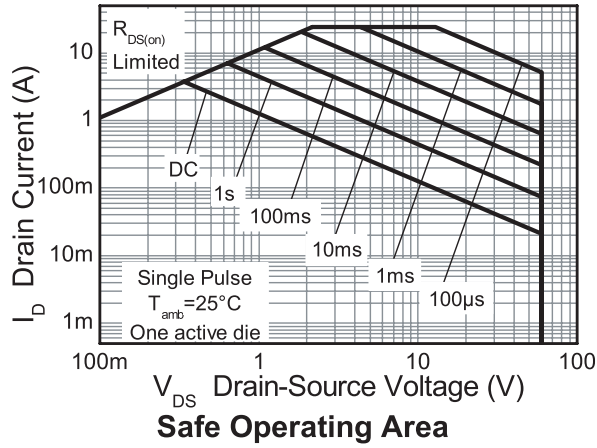
(b) For a device surface mounted on FR4 PCB measured at $t \leq 10$ sec.

(c) Repetitive rating 25mm x 25mm FR4 PCB, $D=0.02$, pulse width=300 μs - pulse width limited by maximum junction temperature.

(d) For a dual device with one active die.

(e) For a device with two active die running at equal power.

Typical characteristics



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Electrical characteristics (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Static						
Drain-source breakdown voltage	$V_{(BR)DSS}$	60			V	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$
Zero gate voltage drain current	I_{DSS}			1.0	mA	$V_{DS}=60\text{V}, V_{GS}=0\text{V}$
Gate-body leakage	I_{GSS}			100	nA	$V_{GS}=\pm 20\text{V}, V_{DS}=0\text{V}$
Gate-source threshold voltage	$V_{GS(th)}$	1.0			V	$I_D=250\mu\text{A}, V_{DS}=V_{GS}$
Static drain-source on-state resistance ^(*)	$R_{DS(on)}$			0.050	Ω	$V_{GS}=10\text{V}, I_D=3.6\text{A}$
				0.070	Ω	$V_{GS}=4.5\text{V}, I_D=3\text{A}$
Forward transconductance ^{(*)(‡)}	g_{fs}		10.2		S	$V_{DS}=15\text{V}, I_D=4.5\text{A}$
Dynamic^(‡)						
Input capacitance	C_{iss}		1063		pF	$V_{DS}=30\text{V},$ $V_{GS}=0\text{V}, f=1\text{MHz}$
Output capacitance	C_{oss}		104		pF	
Reverse transfer capacitance	C_{rss}		64		pF	
Switching^(†) (‡)						
Turn-on delay time	$t_{d(on)}$		3.8		ns	$V_{DD}=30\text{V}, I_D=1\text{A}$ $R_G \cong 6.0\Omega, V_{GS}=10\text{V}$
Rise time	t_r		4.0		ns	
Turn-off delay time	$t_{d(off)}$		26.2		ns	
Fall Time	t_f		10.6		ns	
Gate charge	Q_g		11.0		nC	$V_{DS}=30\text{V}, V_{GS}=5\text{V},$ $I_D=4.5\text{A}$
Total gate charge	Q_g		20.4		nC	$V_{DS}=30\text{V}, V_{GS}=10\text{V},$ $I_D=4.5\text{A}$
Gate-source charge	Q_{gs}		4.1		nC	
Gate-drain charge	Q_{gd}		5.1		nC	
Source-drain diode						
Diode Forward Voltage ^(*)	V_{SD}		0.85	0.95	V	$T_J=25^{\circ}\text{C},$ $I_S=5.5\text{A}, V_{GS}=0\text{V}$
Reverse recovery time ^(‡)	t_{rr}		22.0		ns	$T_J=25^{\circ}\text{C}, I_F=2.2\text{A},$ $di/dt= 100\text{A}/\mu\text{s}$
Reverse recovery charge ^(‡)	Q_{rr}		21.4		nC	

NOTES:

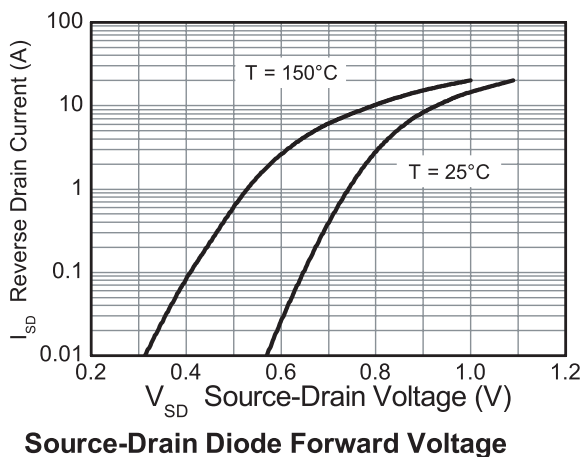
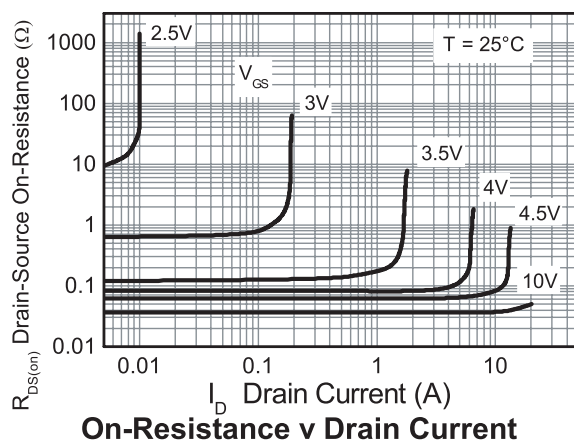
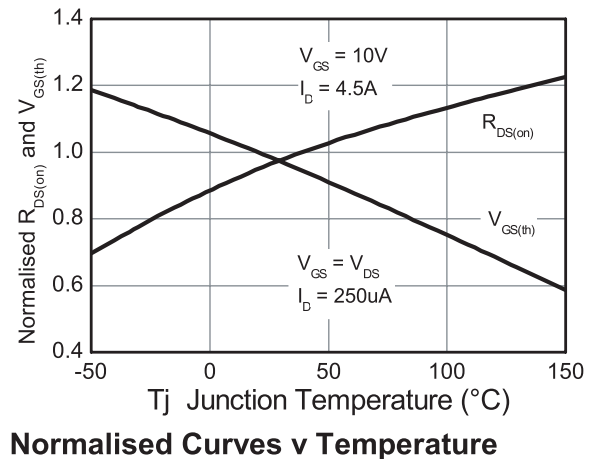
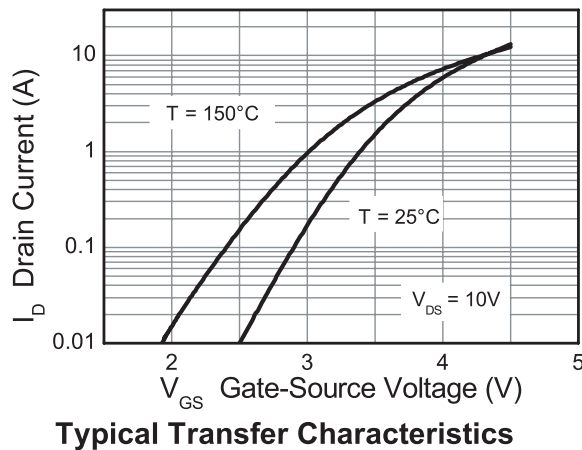
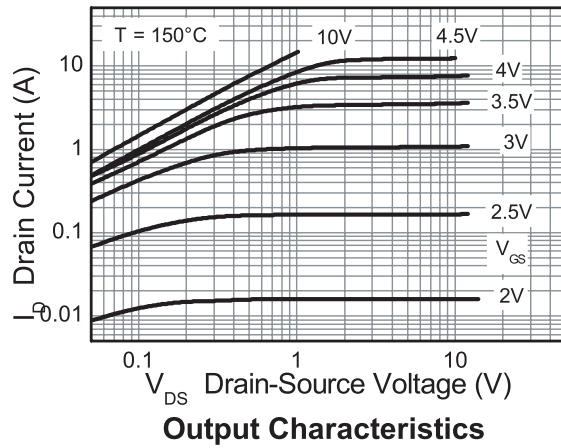
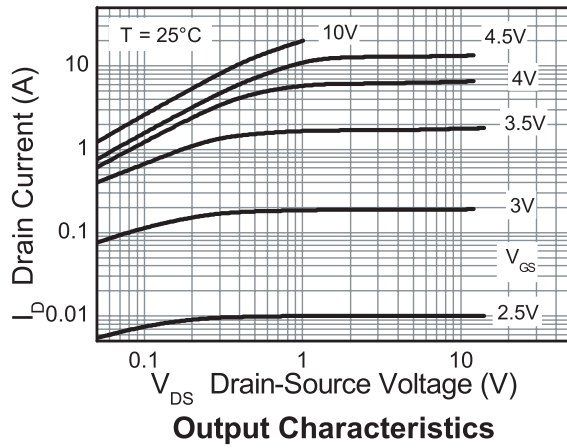
(*) Measured under pulsed conditions. Width=300 μs . Duty cycle $\leq 2\%$.

(†) Switching characteristics are independent of operating junction temperature.

(‡) For design aid only, not subject to production testing.

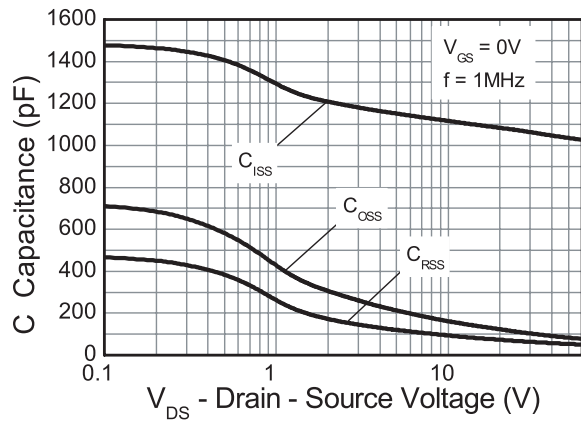
ZXMN6A25DN8

Typical characteristics

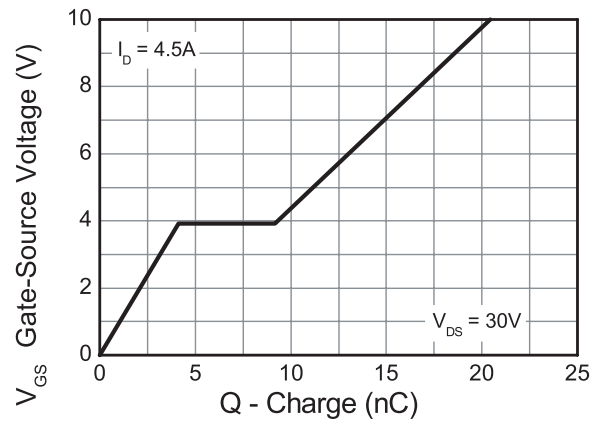


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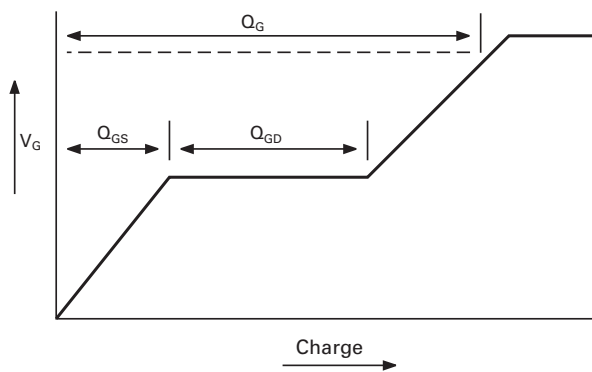
Typical characteristics



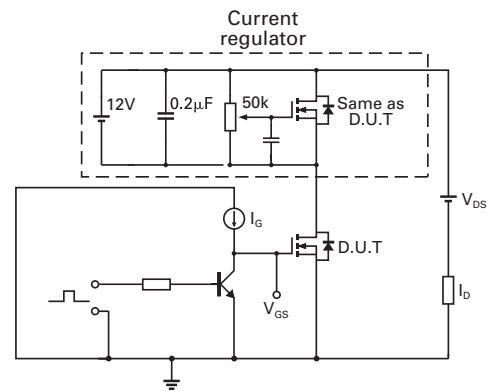
Capacitance v Drain-Source Voltage



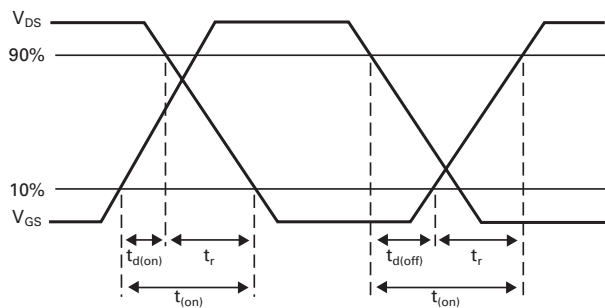
Gate-Source Voltage v Gate Charge



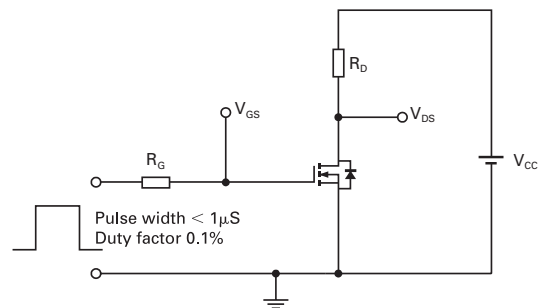
Basic gate charge waveform



Gate charge test circuit



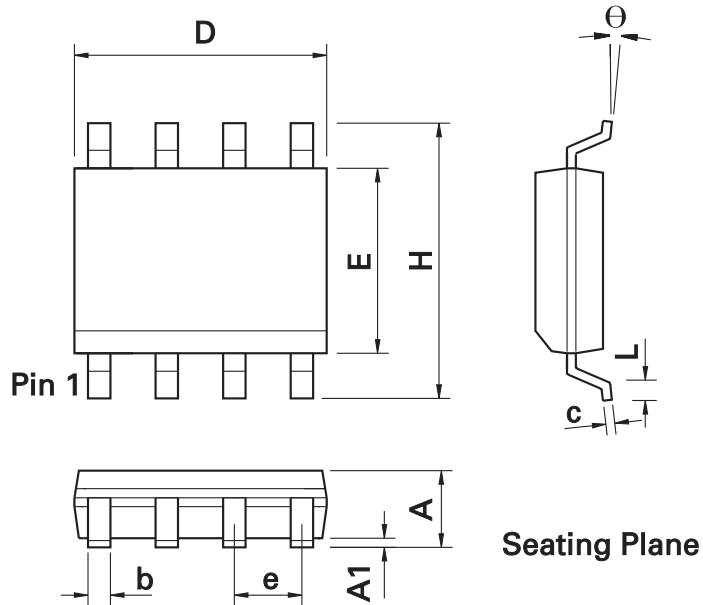
Switching time waveforms



Switching time test circuit

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Package outline - SO8



DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.053	0.069	1.35	1.75	e	0.050 BSC		1.27 BSC	
A1	0.004	0.010	0.10	0.25	b	0.013	0.020	0.33	0.51
D	0.189	0.197	4.80	5.00	c	0.008	0.010	0.19	0.25
H	0.228	0.244	5.80	6.20	Θ	0°	8°	0°	8°
E	0.150	0.157	3.80	4.00	h	0.010	0.020	0.25	0.50
L	0.016	0.050	0.40	1.27	-	-	-	-	-

Note: Controlling dimensions are in inches. Approximate dimensions are provided in millimeters

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