Features

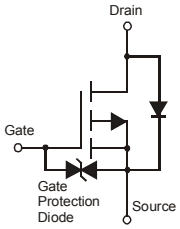
- Low On-Resistance
- Very Low Gate Threshold Voltage $V_{GS(th)}$ < 1V
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- **ESD Protected Gate**
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Mechanical Data

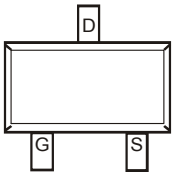
- Case: SOT323
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish — Matte Tin annealed over Alloy 42 leadframe. Solderable per MIL-STD-202, Method 208 e3
- Terminal Connections: See Diagram
- Weight: 0.006 grams (approximate)

SOT323

Top View



Equivalent Circuit



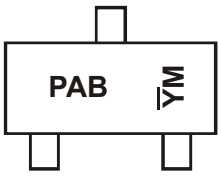
Top View

Ordering Information (Note 4)

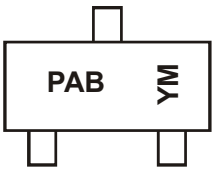
Part Number	Case	Packaging
DMP2004WK-7	SOT323	3000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



Chengdu A/T Site



Shanghai A/T Site

PAB = Product Type Marking Code
YM = Date Code Marking for SAT (Shanghai Assembly/ Test site)
$\overline{Y}M$ = Date Code Marking for CAT (Chengdu Assembly/ Test site)
Y or $\overline{Y}$ = Year (ex: A = 2013)
M = Month (ex: 9 = September)

Date Code Key

Year	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017
Code	U	V	W	X	Y	Z	A	B	C	D	E

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Drain-Source Voltage	V_{DSS}	-20	V
Gate-Source Voltage	V_{GSS}	±8	V
Drain Current (Note 5)	I_D	-400	mA
Pulsed Drain Current	I_{DM}	-1.4	A

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P_d	250	mW
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	500	°C/W
Operating and Storage Temperature Range	T_j, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 6)						
Drain-Source Breakdown Voltage	BV_{DSS}	-20	—	—	V	V_{GS} = 0V, I_D = -250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1.0	µA	V_{DS} = -20V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±1.0	µA	V_{GS} = ±4.5V, V_{DS} = 0V
ON CHARACTERISTICS (Note 6)						
Gate Threshold Voltage	$V_{GS(th)}$	-0.5	—	-1.0	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	0.7 1.1 1.7	0.9 1.4 2.0	Ω	V_{GS} = -4.5V, I_D = -430mA V_{GS} = -2.5V, I_D = -300mA V_{GS} = -1.8V, I_D = -150mA
Forward Transfer Admittance	$\|Y_{fs}\|$	200	—	—	mS	V_{DS} =10V, I_D = -0.2A
Diode Forward Voltage (Note 6)	V_{SD}	-0.5	—	-1.2	V	V_{GS} = 0V, I_S = -115mA
DYNAMIC CHARACTERISTICS (Note 7)						
Input Capacitance	C_{iss}	—	—	175	pF	V_{DS} = -16V, V_{GS} = 0V f = 1.0MHz
Output Capacitance	C_{oss}	—	—	30	pF	
Reverse Transfer Capacitance	C_{rss}	—	—	20	pF	

Notes: 5. Device mounted on FR-4 PCB.
6. Short duration pulse test used to minimize self-heating effect.
7. Guaranteed by design. Not subject to production testing.

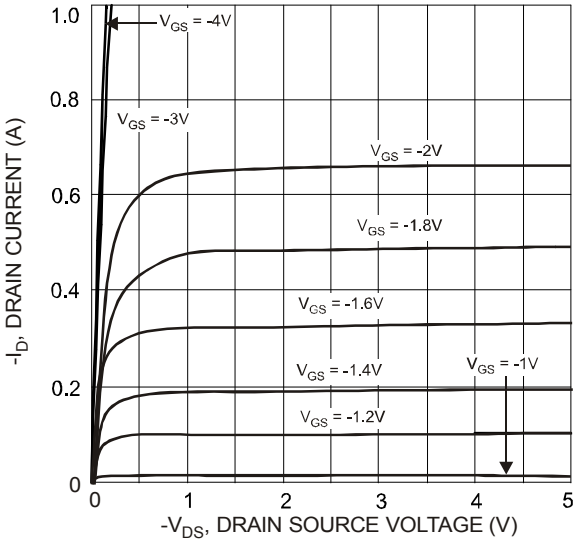


Fig. 1 Typical Output Characteristics

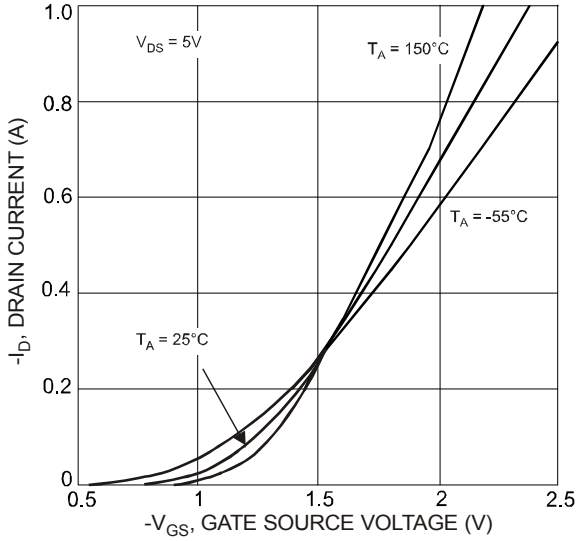


Fig. 2 Typical Transfer Characteristics

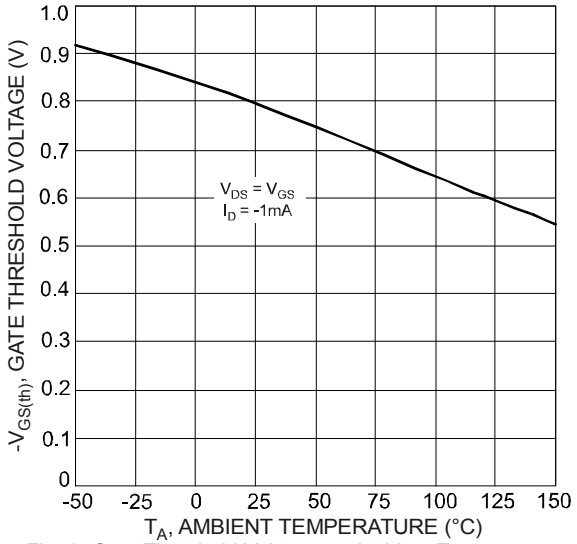


Fig. 3 Gate Threshold Voltage vs. Ambient Temperature

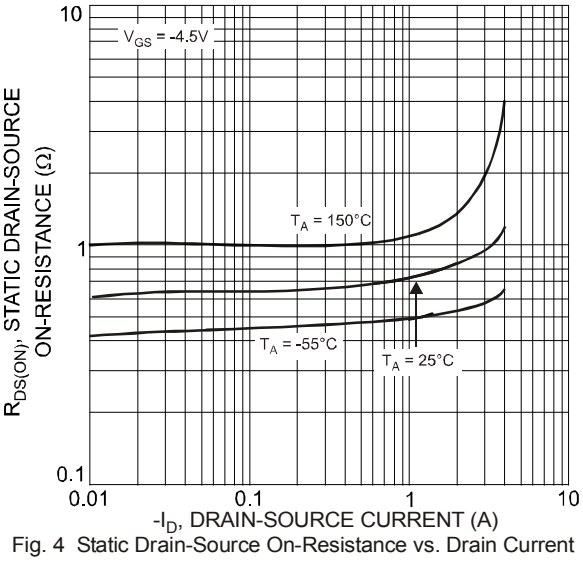


Fig. 4 Static Drain-Source On-Resistance vs. Drain Current

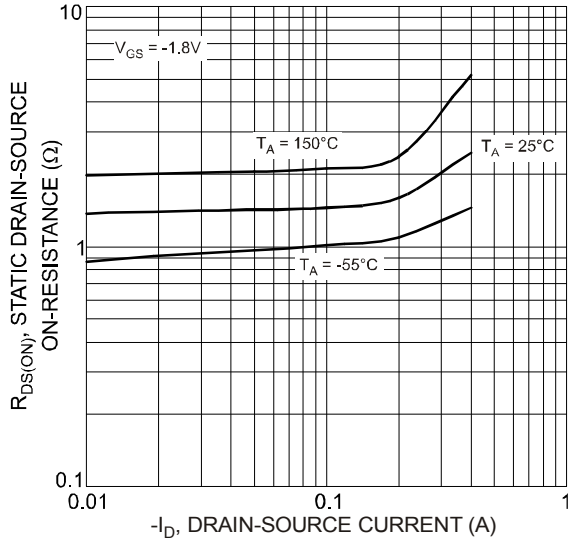


Fig. 5 Static Drain-Source On-Resistance vs. Drain Current

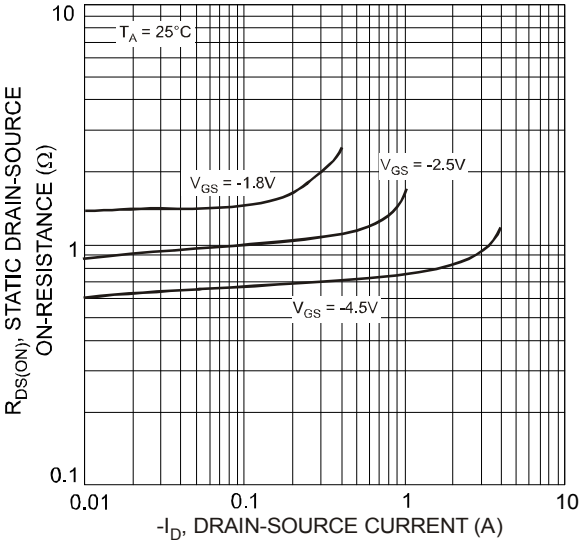


Fig. 6 Static Drain-Source On-Resistance vs. Drain-Source Current vs. Gate Source Voltage

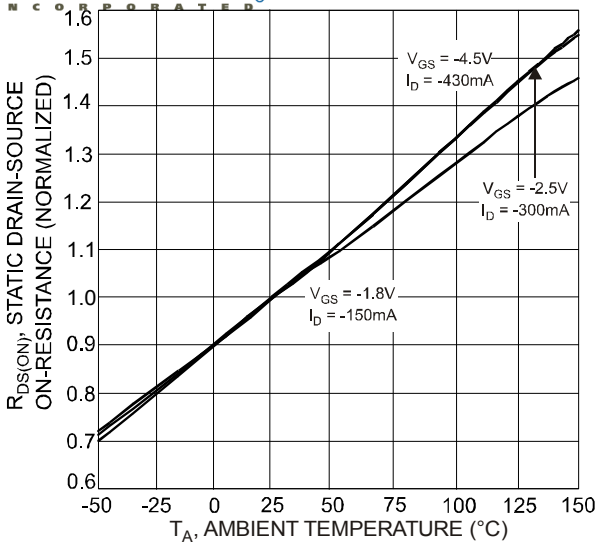


Fig. 7 Static Drain-Source On-State Resistance vs. Ambient Temperature

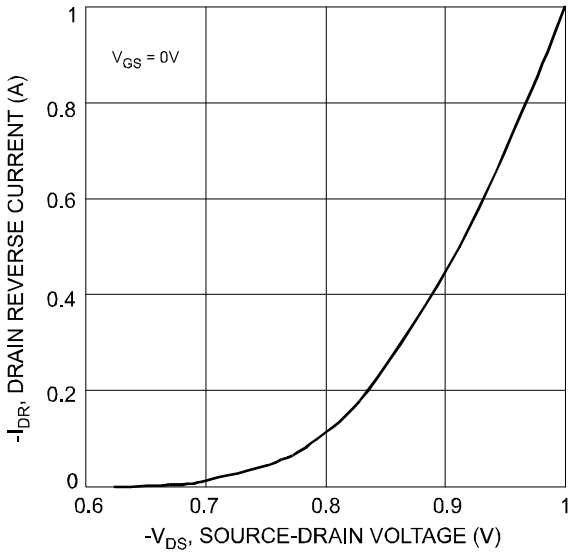


Fig. 8 Drain Reverse Current vs. Source-Drain Voltage

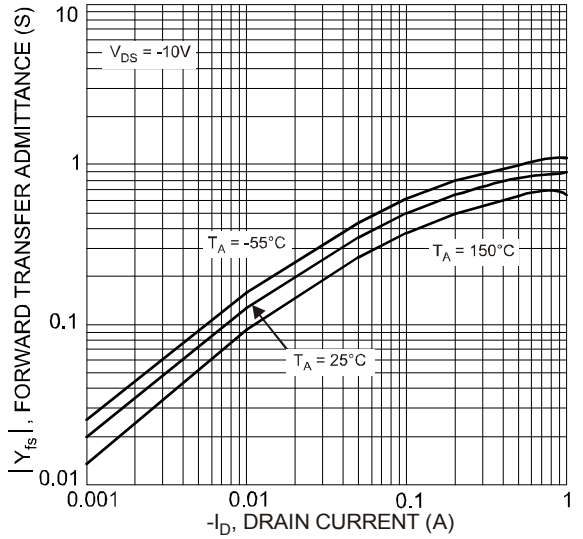


Fig. 9 Forward Transfer Admittance vs. Drain Current

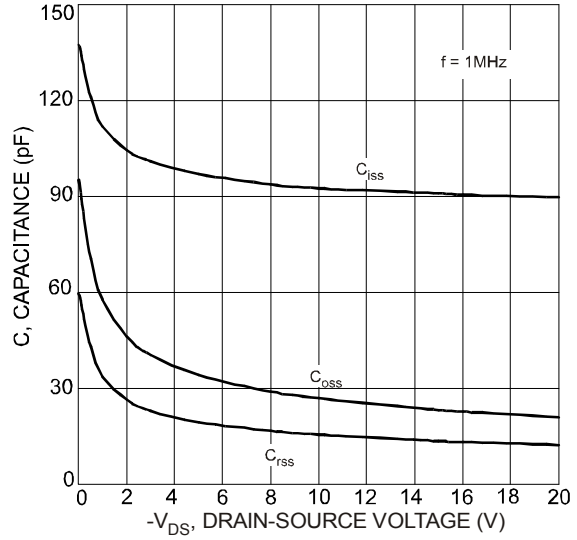
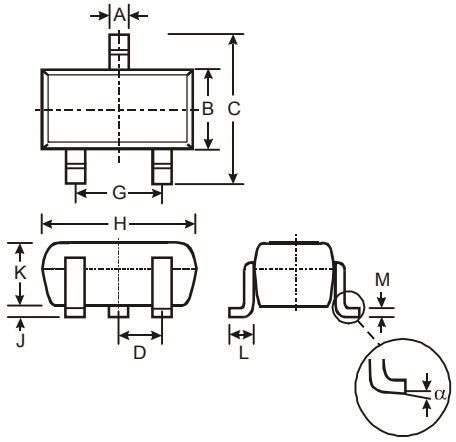


Fig. 10 Typical Capacitance

Package Outline Dimensions

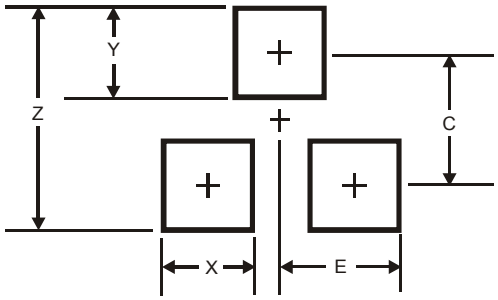
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for latest version.



SOT323			
Dim	**Min**	**Max**	**Typ**
A	0.25	0.40	0.30
B	1.15	1.35	1.30
C	2.00	2.20	2.10
D	-	-	0.65
G	1.20	1.40	1.30
H	1.80	2.20	2.15
J	0.0	0.10	0.05
K	0.90	1.00	0.95
L	0.25	0.40	0.30
M	0.10	0.18	0.11
α	0°	8°	-
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
Z	2.8
X	0.7
Y	0.9
C	1.9
E	1.0

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