

FDI9409_F085

November 2014

N-Channel PowerTrench® MOSFET

40 V, 80 A, 3.8 mΩ

Features

- Typical $R_{DS(on)}$ = 2.9 m Ω at V_{GS} = 10V, I_D = 80 A
- Typical $Q_{q(tot)}$ = 43 nC at V_{GS} = 10V, I_D = 80 A
- UIS Capability
- RoHS Compliant
- Qualified to AEC Q101

Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12V Systems



For current package drawing, please refer to the Fairchild website at https://www.fairchildsemi.com/package-drawings/TO/TO262A03.pdf

I²-PAK

(TO-262)

MOSFET Maximum Ratings T_J = 25°C unless otherwise noted.

Symbol	Parameter		Ratings	Units	
V_{DSS}	Drain-to-Source Voltage		40	V	
V_{GS}	Gate-to-Source Voltage		±20	V	
	Drain Current - Continuous (V_{GS} =10) (Note 1) T_C = 25°C		80	^	
ID	Pulsed Drain Current T _C = 25°C		See Figure 4	A	
E _{AS}	Single Pulse Avalanche Energy (Note 2)		70	mJ	
D	Power Dissipation		94	W	
P_D	Derate Above 25°C		0.63	W/°C	
T _J , T _{STG}	Operating and Storage Temperature		-55 to + 175	°C	
$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.6	°C/W	
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)		43	°C/W	

GDS

Notes

- 1: Current is limited by bondwire configuration.
- 2: Starting $T_J = 25^{\circ}C$, L = 34uH, $I_{AS} = 64A$, $V_{DD} = 40V$ during inductor charging and $V_{DD} = 0V$ during time in avalanche.
- 3: R_{0,JA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{0,JC} is guaranteed by design, while R_{0,JA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDI9409	FDI9409_F085	TO-262	Tube	N/A	50 units

Max.

Min.

Тур.

Units

Electrical Characteristics $T_J = 25^{\circ}C$ unless otherwise noted.

Parameter

Off Characteristics								
B _{VDSS}	Drain-to-Source Breakdown Voltage	$I_D = 250 \mu A$,	V _{GS} = 0V	40	-	-	V	
I _{DSS}	Drain-to-Source Leakage Current	V _{DS} =40V,	$T_J = 25^{\circ}C$	-	-	1	μА	
		$V_{GS} = 0V$	$T_J = 175^{\circ}C \text{ (Note 4)}$	-	-	1	mA	
loss	Gate-to-Source Leakage Current	$V_{CS} = +20V$, i	-	_	+100	nΑ	

Test Conditions

On Characteristics

Symbol

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$		2.0	3.0	4.0	V
R _{DS(op)} Drain to Source On Resistance	I _D = 80A,	$T_{J} = 25^{\circ}C$	-	2.9	3.8	$m\Omega$	
NDS(on)	R _{DS(on)} Drain to Source On Resistance	V _{GS} = 10V	$T_J = 175^{\circ}C \text{ (Note 4)}$	-	4.9	6.4	mΩ

Dynamic Characteristics

C _{iss}	Input Capacitance	V 05.V.V	V _{DS} = 25 V, V _{GS} = 0V, f = 1MHz		2980	-	pF
C _{oss}	Output Capacitance				788	-	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1101112			45	-	pF
R_g	Gate Resistance	f = 1MHz	f = 1MHz		2.2	-	Ω
$Q_{g(ToT)}$	Total Gate Charge at 10V	$V_{GS} = 0$ to 10V	V _{DD} = 32V	-	43	56	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0$ to 2V	$V_{GS} = 0 \text{ to } 2V$ $I_D = 80A$		5	7	nC
Q_{gs}	Gate-to-Source Gate Charge				15.5	-	nC
Q_{ad}	Gate-to-Drain "Miller" Charge			-	10	-	nC

Switching Characteristics

t _{on}	Turn-On Time		-	-	193	ns
$t_{d(on)}$	Turn-On Delay		-	17	1	ns
t _r	Rise Time	V_{DD} = 20V, I_{D} = 80A, V_{GS} = 10V, R_{GEN} = 6 Ω	-	90	-	ns
t _{d(off)}	Turn-Off Delay		-	24	-	ns
t _f	Fall Time		-	10	-	ns
t _{off}	Turn-Off Time		-	ı	50	ns

Drain-Source Diode Characteristics

Ven Source-to-Drain Dioge Voltage	Source to Drain Diade Voltage	I _{SD} =80A, V _{GS} = 0V	-	-	1.25	V
	$I_{SD} = 40A, V_{GS} = 0V$	-	-	1.2	V	
t _{rr}	Reverse-Recovery Time	I _F = 80A, dI _{SD} /dt = 100A/μs,	-	54	71	ns
Q _{rr}	Reverse-Recovery Charge	V _{DD} =32V	-	47	62	nC

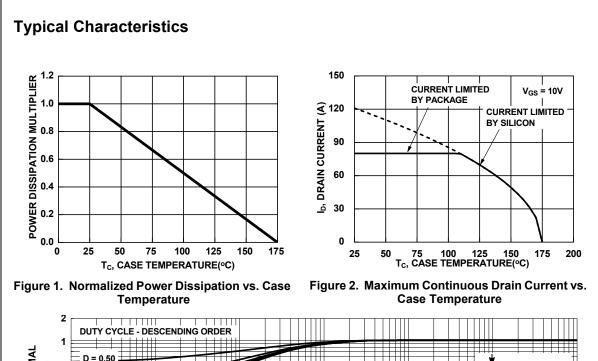
Note

4: The maximum value is specified by design at T_J = 175°C. Product is not tested to this condition in production.

150

10¹

10°



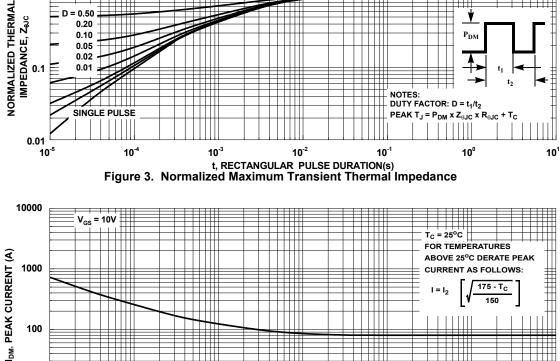


Figure 4. Peak Current Capability

10⁻²

t, RECTANGULAR PULSE DURATION(s)

10⁻³

10⁻¹

100

10 10⁻⁵ SINGLE PULSE

10⁴

Typical Characteristics

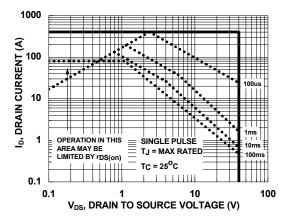
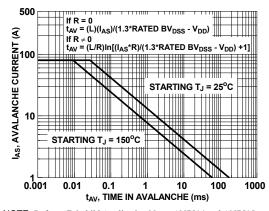


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

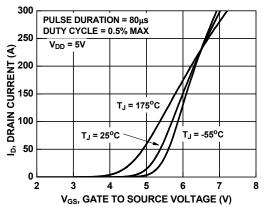


Figure 7. Transfer Characteristics

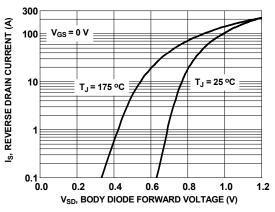


Figure 8. Forward Diode Characteristics

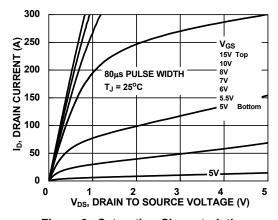


Figure 9. Saturation Characteristics

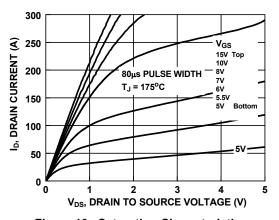


Figure 10. Saturation Characteristics

Typical Characteristics

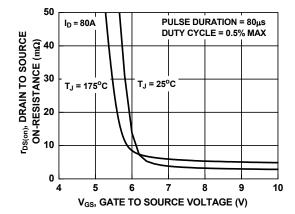


Figure 11. R_{DSON} vs. Gate Voltage

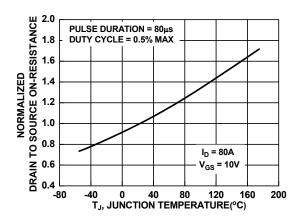


Figure 12. Normalized R_{DSON} vs. Junction Temperature

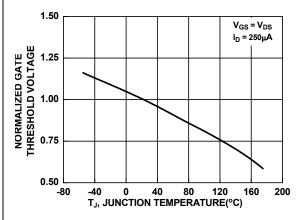


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

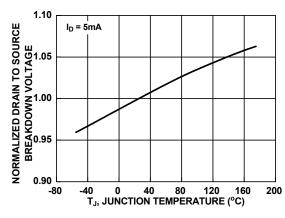


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

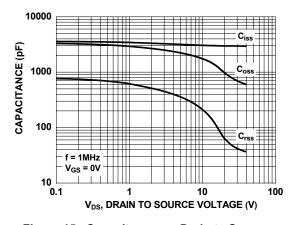


Figure 15. Capacitance vs. Drain to Source Voltage

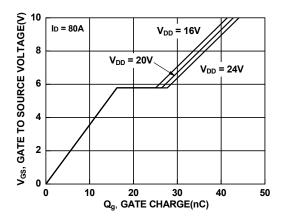


Figure 16. Gate Charge vs. Gate to Source Voltage





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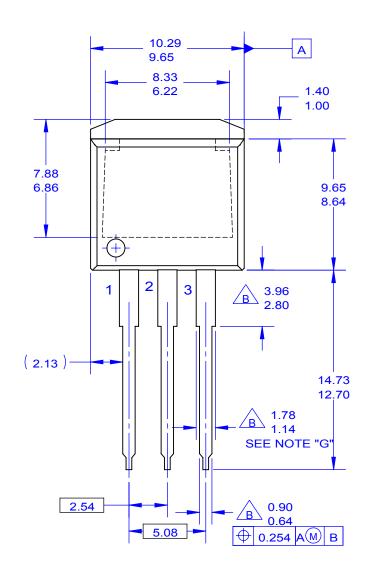
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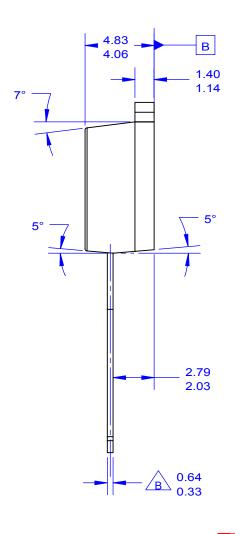
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C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS,
MOLD FLASH AND TIE BAR PROTRUSIONS.
E. DIMENSION AND TOLERANCE AS PER ANSI
Y14 5-1904

Y14.5-1994

F. LOCATION OF PIN HOLE MAY VARY
(LOWER LEFT CORNER, LOWER CENTER
AND CENTER OF PACKAGE)
G. MAXIMUM WIDTH FOR F102 DEVICE = 1.35 MAX.
H. DRAWING FILE NAME: TO262A03REV6







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