June 2014

FDMC8622

N-Channel Shielded Gate PowerTrench® MOSFET
100 V, 16 A, 56 mΩ

Features

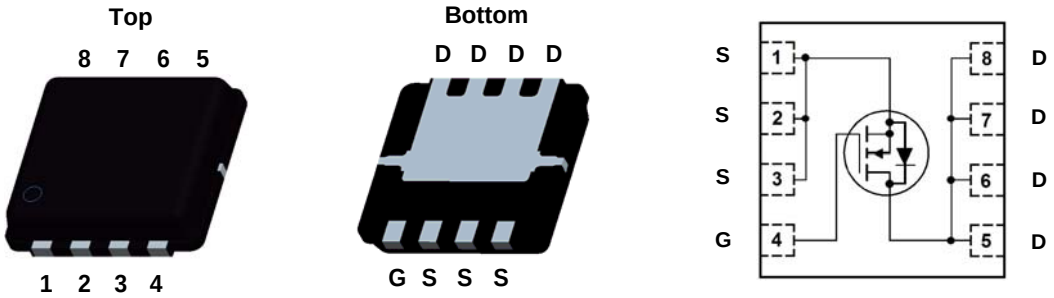
- Shielded Gate MOSFET Technology
- Max $r_{DS(on)}$ = 56 mΩ at V_{GS} = 10 V, I_D = 4 A
- Max $r_{DS(on)}$ = 90 mΩ at V_{GS} = 6 V, I_D = 3 A
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- 100% UIL Tested
- Termination is Lead-free and RoHS Compliant

General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that incorporates Shielded Gate technology. This process has been optimized for $r_{DS(on)}$, switching performance and ruggedness.

Application

- DC-DC Primary Switch



MLP 3.3X3.3

MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			100	V
V_{GS}	Gate to Source Voltage			±20	V
I_D	Drain Current -Continuous	T_C = 25 °C		16	A
	-Continuous	T_A = 25 °C	(Note 1a)	4	
	-Pulsed		(Note 4)	30	
E_{AS}	Single Pulse Avalanche Energy		(Note 3)	37	mJ
P_D	Power Dissipation	T_C = 25 °C		31	W
	Power Dissipation	T_A = 25 °C	(Note 1a)	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	4.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	53	

Package Marking and Ordering Information

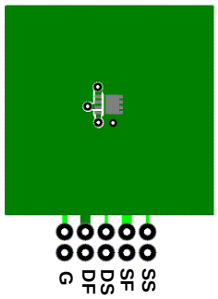
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC8622	FDMC8622	MLP 3.3X3.3	13 "	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

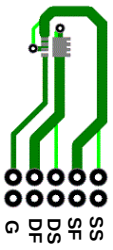
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		69		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2	2.9	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		-9		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 4 A		43.7	56	mΩ
		V_{GS} = 6 V, I_D = 3 A		59.9	90	
		V_{GS} = 10 V, I_D = 4 A, T_J = 125 °C		76.4	98	
g_{FS}	Forward Transconductance	V_{DD} = 10 V, I_D = 4 A		8.9		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		302	402	pF
C_{oss}	Output Capacitance			72.5	96	pF
C_{rss}	Reverse Transfer Capacitance			4.2	6	pF
R_g	Gate Resistance			1.0		Ω
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 50 V, I_D = 4 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		5.9	12	ns
t_r	Rise Time			1.6	10	ns
$t_{d(off)}$	Turn-Off Delay Time			10.2	18	ns
t_f	Fall Time			2.2	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; V_{DD} = 50 V, I_D = 4 A		5.2	7.3	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 5 V; V_{DD} = 50 V, I_D = 4 A		3.0	4.1	nC
Q_{gs}	Total Gate Charge	V_{DD} = 50 V, I_D = 4 A		1.4		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = 50 V, I_D = 4 A		1.4		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 4 A (Note 2)		0.8	1.3	V
		V_{GS} = 0 V, I_S = 1.7 A (Note 2)		0.8	1.2	
t_{rr}	Reverse Recovery Time	I_F = 4 A, di/dt = 100 A/μs		36	57	ns
Q_{rr}	Reverse Recovery Charge			28	45	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 125 °C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. Starting T_J = 25 °C; N-ch: L = 3.0 mH, I_{AS} = 5.0 A, V_{DD} = 100 V, V_{GS} = 10 V.

4. Pulse Id refers to Figure.11 Forward Bias Safe Operation Area.

Typical Characteristics T_J = 25°C unless otherwise noted

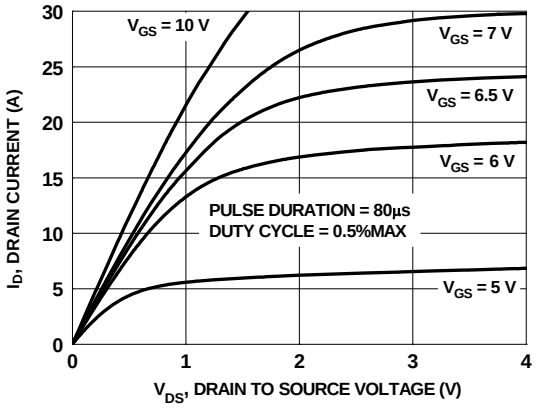


Figure 1. On-Region Characteristics

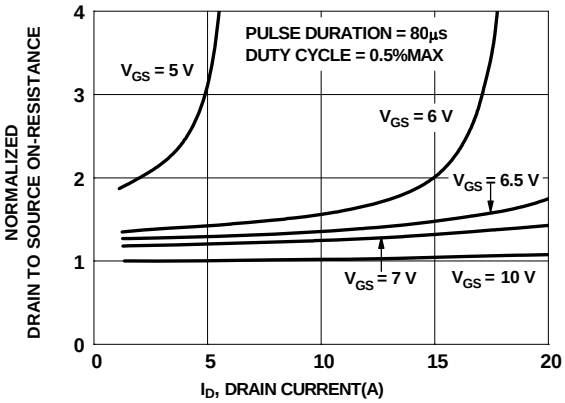


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

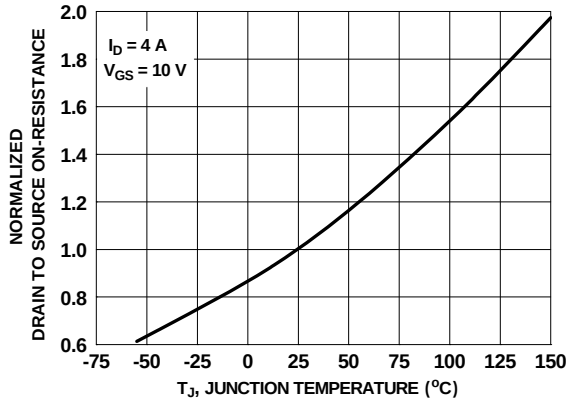


Figure 3. Normalized On-Resistance vs Junction Temperature

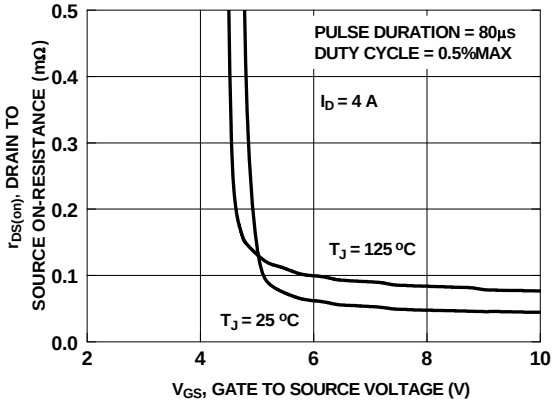


Figure 4. On-Resistance vs Gate to Source Voltage

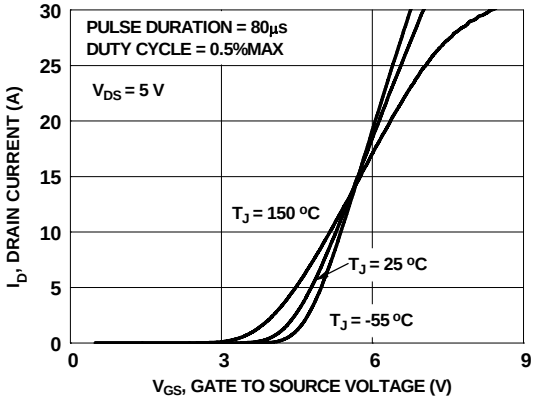


Figure 5. Transfer Characteristics

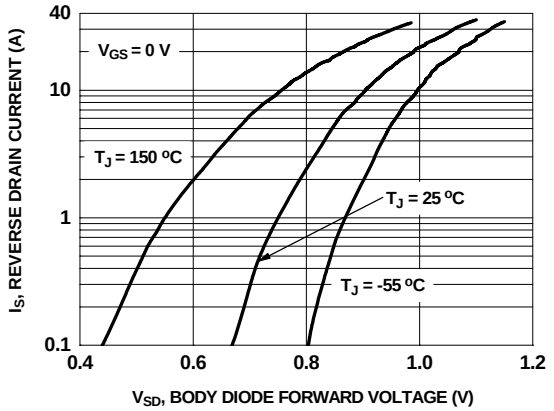


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25°C unless otherwise noted

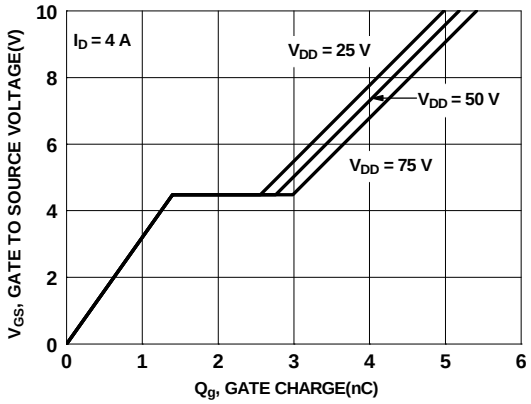


Figure 7. Gate Charge Characteristics

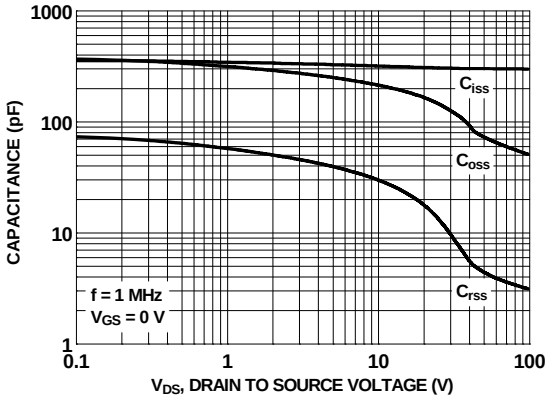


Figure 8. Capacitance vs Drain to Source Voltage

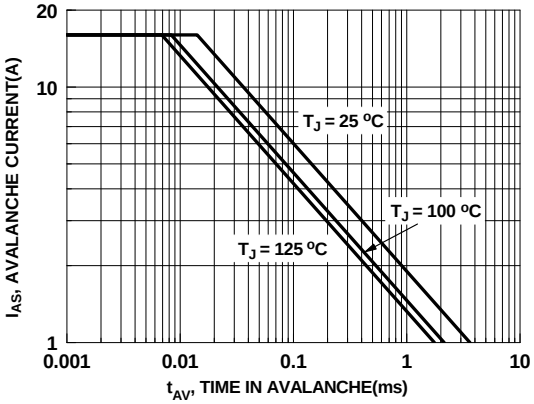


Figure 9. Unclamped Inductive Switching Capability

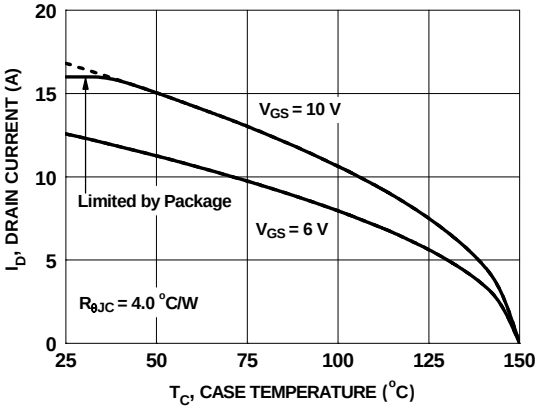


Figure 10. Maximum Continuous Drain Current vs Case Temperature

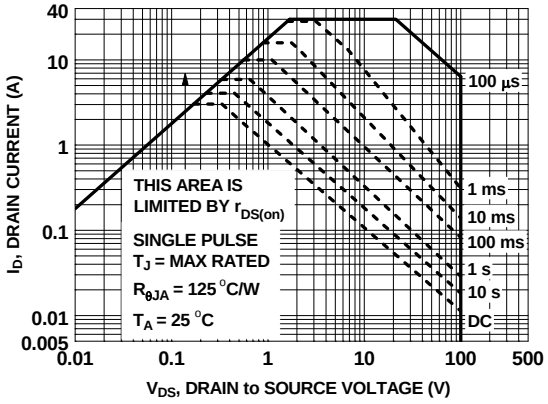


Figure 11. Forward Bias Safe Operating Area

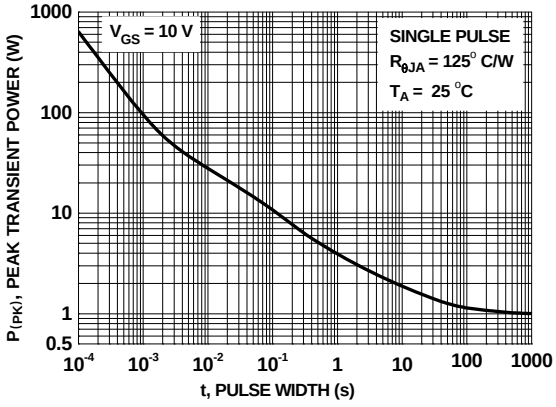


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25°C unless otherwise noted

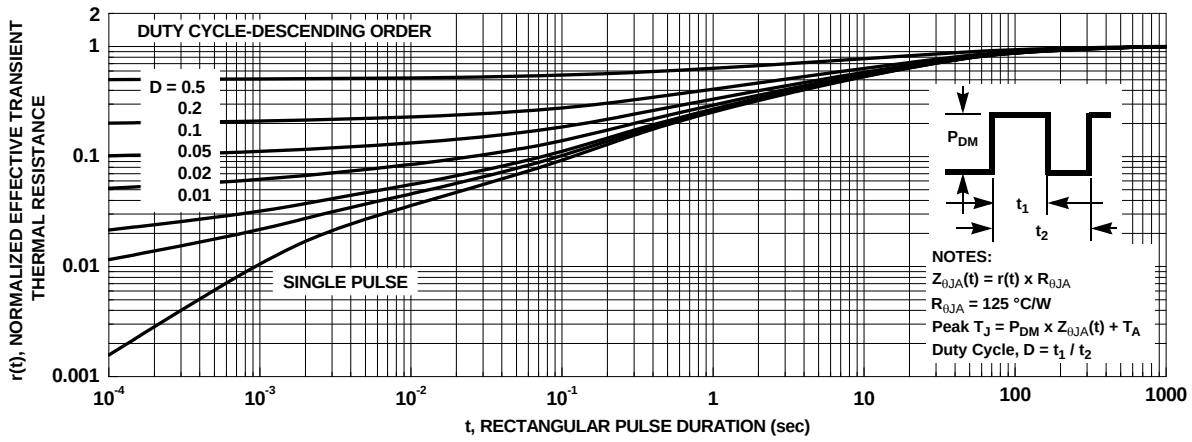
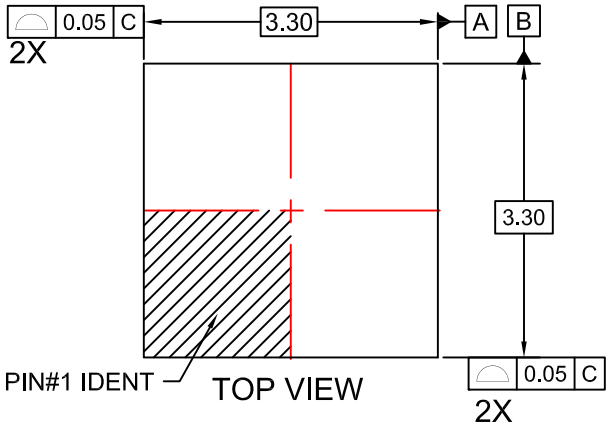
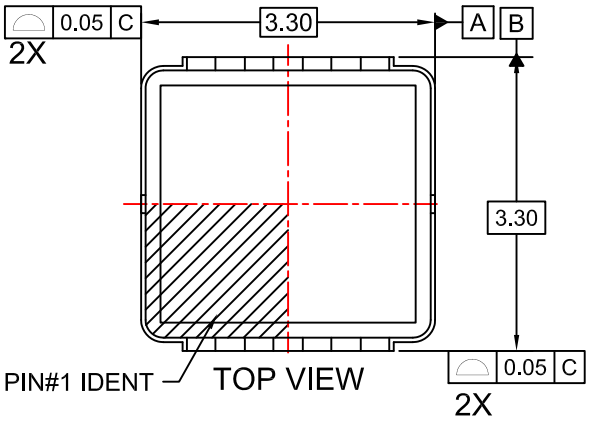
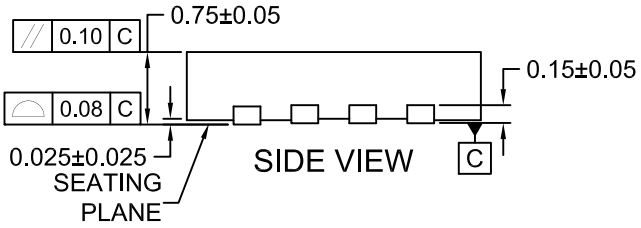
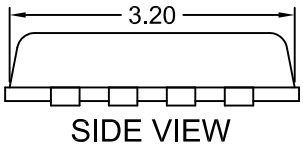


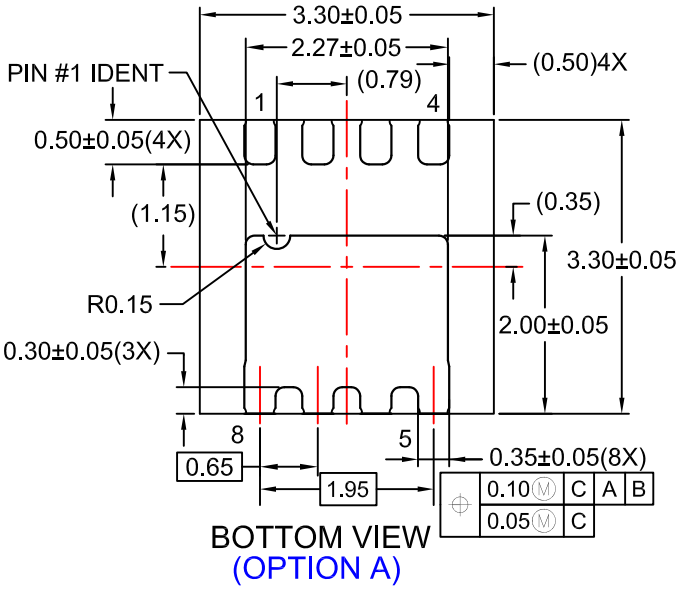
Figure 13. Junction-to-Ambient Transient Thermal Response Curve

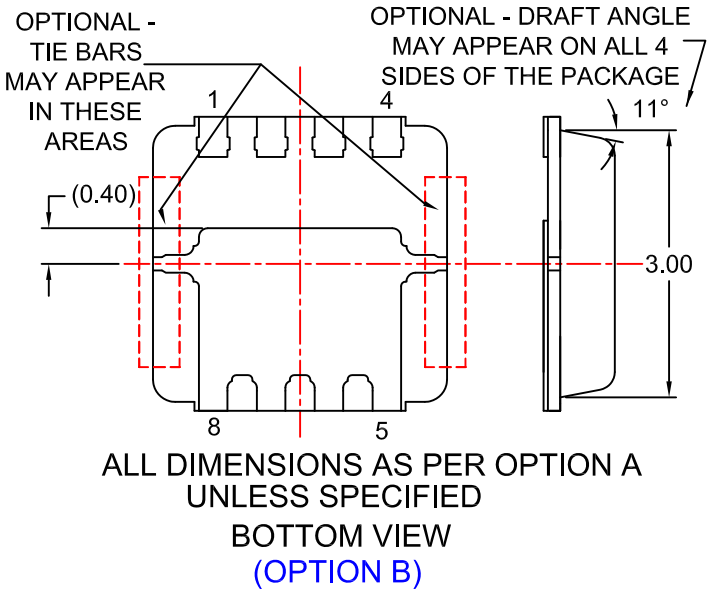

0.05 C
2X
3.30
A
B
3.30
PIN#1 IDENT
TOP VIEW
0.05 C
2X

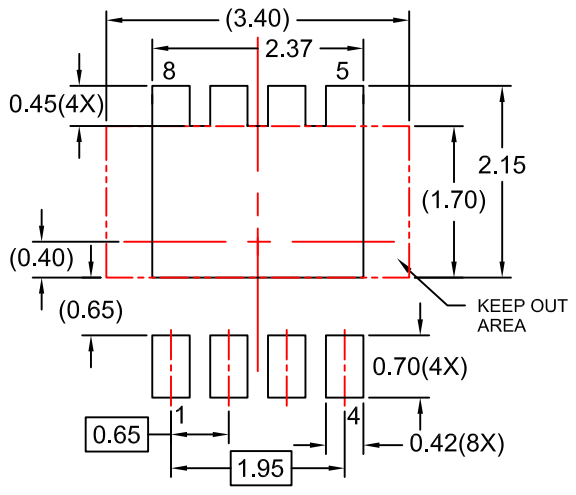

0.05 C
2X
3.30
A
B
3.30
PIN#1 IDENT
TOP VIEW
0.05 C
2X


0.10 C
0.75±0.05
0.08 C
0.15±0.05
0.025±0.025
SEATING
PLANE
SIDE VIEW
C

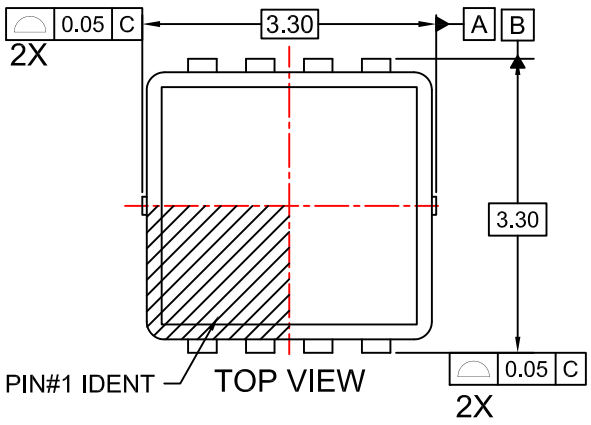

3.20
SIDE VIEW

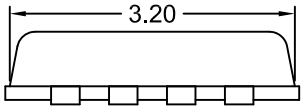

3.30±0.05
2.27±0.05
(0.79)
(0.50)4X
PIN #1 IDENT
1
4
0.50±0.05(4X)
(1.15)
(0.35)
3.30±0.05
R0.15
2.00±0.05
0.30±0.05(3X)
8
5
0.65
1.95
0.35±0.05(8X)
0.10 M C A B
0.05 M C
BOTTOM VIEW
(OPTION A)


OPTIONAL -
TIE BARS
MAY APPEAR
IN THESE
AREAS
OPTIONAL - DRAFT ANGLE
MAY APPEAR ON ALL 4
SIDES OF THE PACKAGE
1
4
11°
(0.40)
3.00
8
5
ALL DIMENSIONS AS PER OPTION A
UNLESS SPECIFIED
BOTTOM VIEW
(OPTION B)

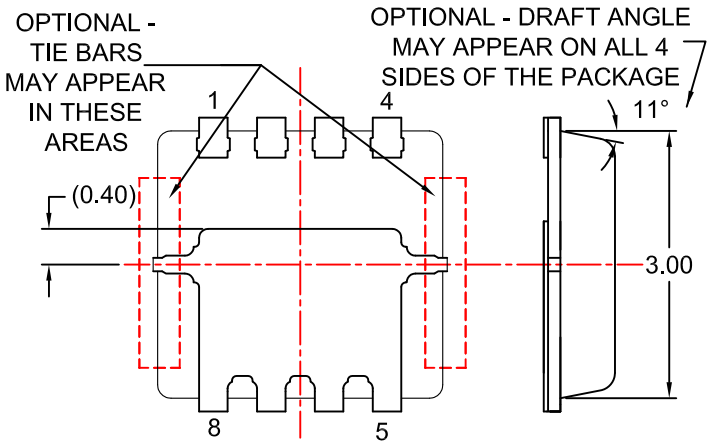

(3.40)
2.37
8
5
0.45(4X)
2.15
(1.70)
(0.40)
(0.65)
KEEP OUT
AREA
0.70(4X)
0.65
1
4
0.42(8X)
1.95
RECOMMENDED LAND PATTERN

FAIRCHILD.





SIDE VIEW



ALL DIMENSIONS AS PER OPTION A
UNLESS SPECIFIED

BOTTOM VIEW
(OPTION C)

NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-240.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN
E. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. BURRS OR MOLD FLASH SHALL NOT EXCEED 0.10MM.
F. DRAWING FILENAME: MKT-MLP08Wrev3.
G. OPTION A - SAWN MLP, OPTIONS B & C - PUNCH MLP.

FAIRCHILD.

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Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I77

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