May 2014

FDMS9600S

Dual N-Channel PowerTrench® MOSFET

Q1: 30V, 32A, 8.5mΩ Q2: 30V, 30A, 5.5mΩ

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 8.5mΩ at V_{GS} = 10V, I_D = 12A
- Max $r_{DS(on)}$ = 12.4mΩ at V_{GS} = 4.5V, I_D = 10A

Q2: N-Channel

- Max $r_{DS(on)}$ = 5.5mΩ at V_{GS} = 10V, I_D = 16A
- Max $r_{DS(on)}$ = 7.0mΩ at V_{GS} = 4.5V, I_D = 14A
- Low Qg high side MOSFET
- Low $r_{DS(on)}$ low side MOSFET
- Thermally efficient dual Power 56 package
- Pinout optimized for simple PCB design
- RoHS Compliant

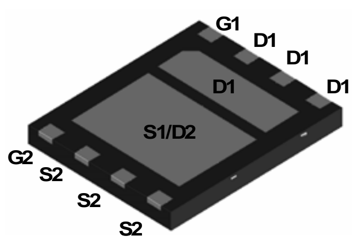
General Description

This device includes two specialized MOSFETs in a unique dual Power 56 package. It is designed to provide an optimal Synchronous Buck power stage in terms of efficiency and PCB utilization. The low switching loss "High Side" MOSFET is complemented by a Low Conduction Loss "Low Side" SyncFET.

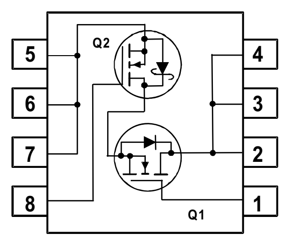
Applications

Synchronous Buck Converter for:

- Notebook System Power
- General Purpose Point of Load



Power 56



MOSFET Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter			Q1	Q2	Units
V_{DS}	Drain to Source Voltage			30	30	V
V_{GS}	Gate to Source Voltage			±20	±20	V
I_D	Drain Current -Continuous	T_C = 25°C		32	30	A
	-Continuous	T_A = 25°C	(Note 1a)	12	16	
	-Pulsed			60	60	
P_D	Power Dissipation for Single Operation		(Note 1a)	2.5		W
			(Note 1b)	1.0		
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150		°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1b)	120		
$R_{\theta JC}$	Thermal Resistance, Junction to Case		3	1.2	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS9600S	FDMS9600S	Power 56	13”	12mm	3000 units

Electrical Characteristics T_J = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V I_D = 1mA, V_{GS} = 0V	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C I_D = 1mA, referenced to 25°C	Q1 Q2		35 29		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24V, V_{GS} = 0V	Q1 Q2			1 500	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20V, V_{DS}= 0V	Q1 Q2			±100 ±100	nA nA
On Characteristics							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA V_{GS} = V_{DS}, I_D = 1mA	Q1 Q2	1 1	1.5 1.8	3 3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250μA, referenced to 25°C I_D = 1mA, referenced to 25°C	Q1 Q2		-4.5 -6.0		mV/°C
$r_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 10V, I_D = 12A V_{GS} = 4.5V, I_D = 10A V_{GS} = 10V, I_D = 12A , T_J = 125°C	Q1		7.0 9.2 8.6	8.5 12.4 13.0	mΩ
		V_{GS} = 10V, I_D = 16A V_{GS} = 4.5V, I_D = 14A V_{GS} = 10V, I_D = 16A , T_J = 125°C	Q2		4.5 5.3 5.4	5.5 7.0 8.3	
g_{FS}	Forward Transconductance	V_{DD} = 10V, I_D = 12A V_{DD} = 10V, I_D = 16A	Q1 Q2		54 68		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	V_{DS} = 15V, V_{GS} = 0V, f= 1MHz	Q1 Q2		1280 2300	1705 3060	pF
C_{oss}	Output Capacitance		Q1 Q2		525 1545	700 2055	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2		80 250	120 375	pF
R_g	Gate Resistance	f = 1MHz	Q1 Q2		1.0 1.7		Ω
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 10V, I_D = 1A, V_{GS} = 10V, R_{GEN} = 6Ω	Q1 Q2		13 17	23 31	ns
t_r	Rise Time		Q1 Q2		6 11	12 20	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		42 54	67 86	ns
t_f	Fall Time		Q1 Q2		12 32	22 51	ns
$Q_{g(TOT)}$	Total Gate Charge	Q1 V_{DD} = 15V, V_{GS} = 4.5V, I_D = 12A Q2 V_{DD} = 15V, V_{GS} = 4.5V, I_D = 16A	Q1 Q2		9 21	13 29	nC
Q_{gs}	Gate to Source Gate Charge		Q1 Q2		3 8		nC
Q_{gd}	Gate to Drain "Miller" Charge		Q1 Q2		2.7 6.5		nC

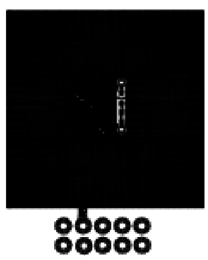
Electrical Characteristics T_J = 25°C unless otherwise noted

Drain-Source Diode Characteristics

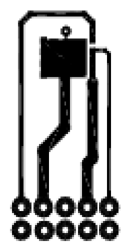
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q1 Q2			2.1 3.5	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0V, I_S = 2.1A (Note 2) V_{GS} = 0V, I_S = 3.5A (Note 2) V_{GS} = 0V, I_S = 8.2A (Note 2)	Q1 Q2 Q2		0.7 0.4 0.5	1.2 1.0 1.0	V
t_{rr}	Reverse Recovery Time	Q1 I_F = 12A, di/dt = 100A/μs	Q1 Q2		33 27		ns
Q_{rr}	Reverse Recovery Charge	Q2 I_F = 16A, di/dt = 300A/μs	Q1 Q2		20 33		nC

Notes:

1: $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a.50°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 120°C/W when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

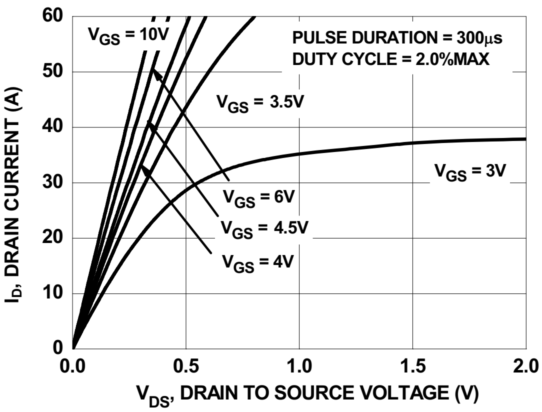


Figure 1. On-Region Characteristics

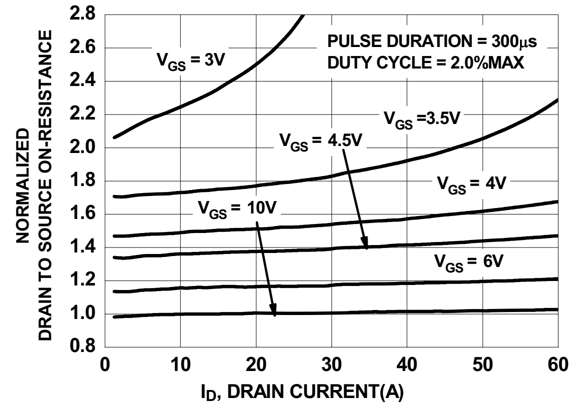


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

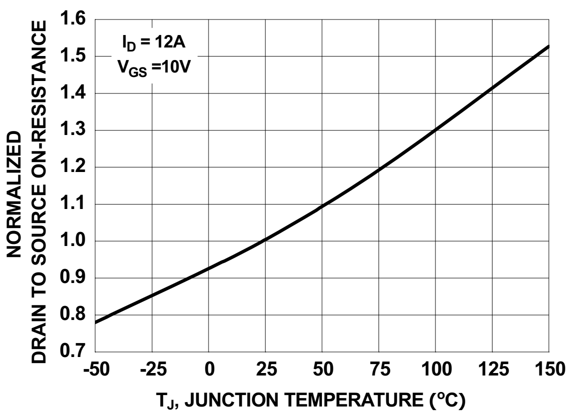


Figure 3. Normalized On-Resistance vs Junction Temperature

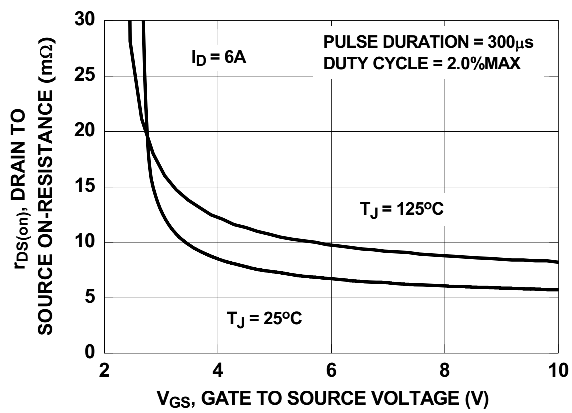


Figure 4. On-Resistance vs Gate to Source Voltage

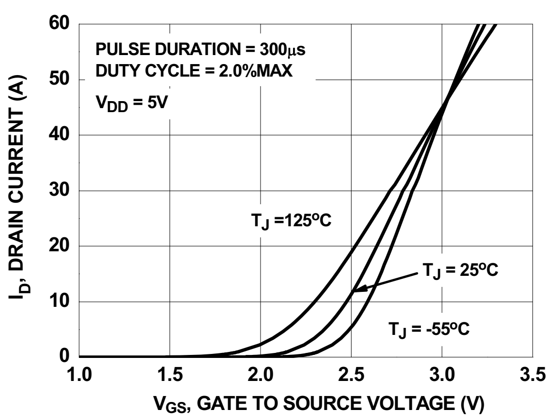


Figure 5. Transfer Characteristics

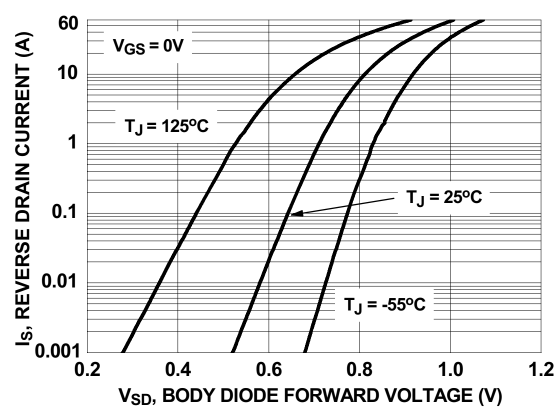


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) T_J = 25°C unless otherwise noted

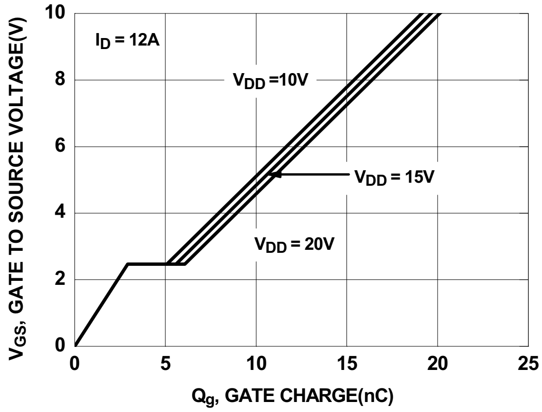


Figure 7. Gate Charge Characteristics

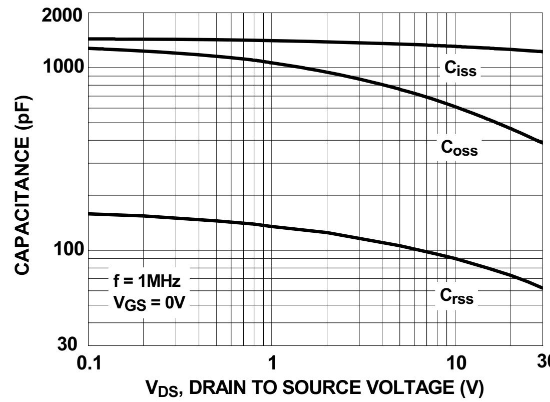


Figure 8. Capacitance vs Drain to Source Voltage

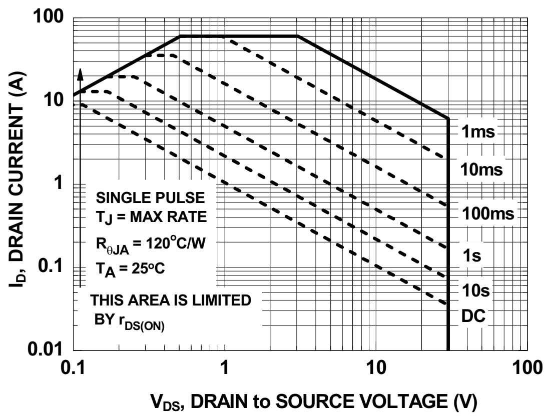


Figure 9. Forward Bias Safe Operating Area

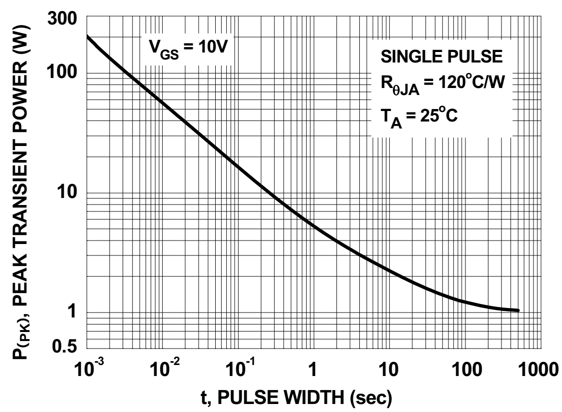


Figure 10. Single Pulse Maximum Power Dissipation

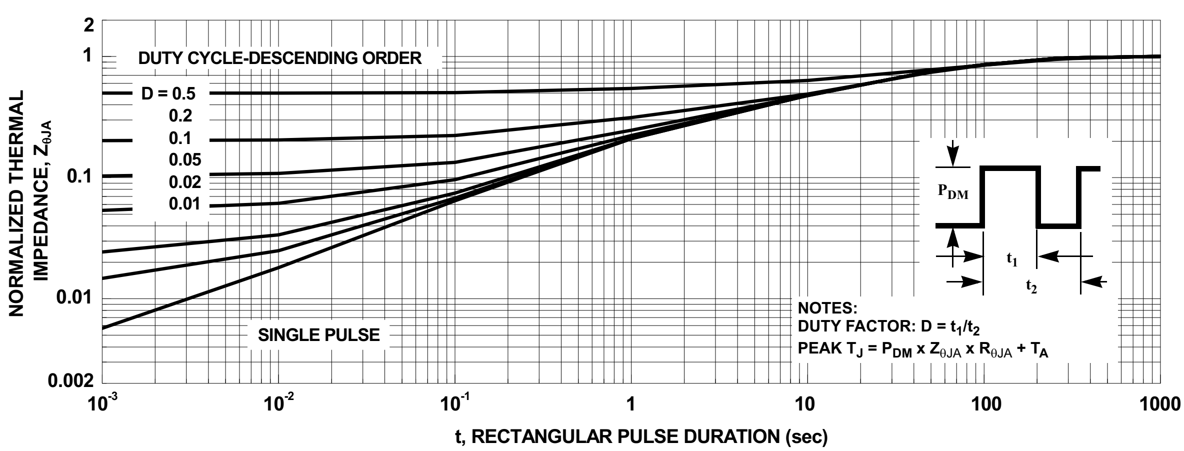


Figure 11. Transient Thermal Response Curve

Typical Characteristics (Q2 SyncFET)

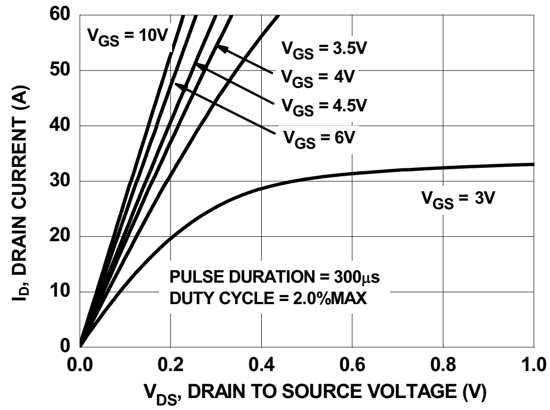


Figure 12. On-Region Characteristics

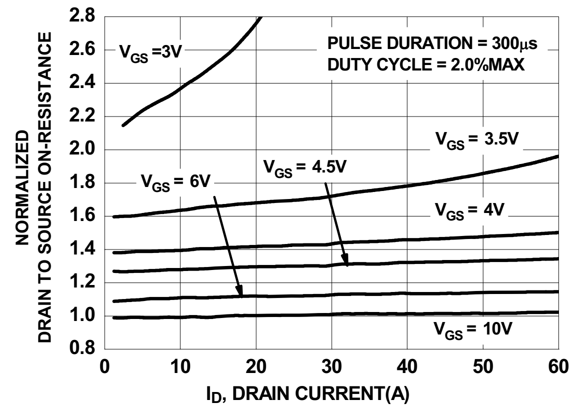


Figure 13. Normalized on-Resistance vS Drain Current and Gate Voltage

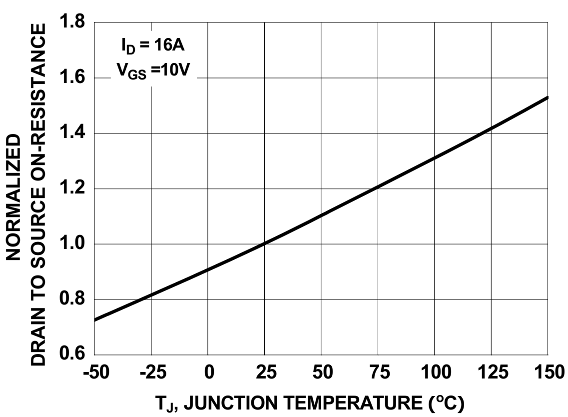


Figure 14. Normalized On-Resistance vs Junction Temperature

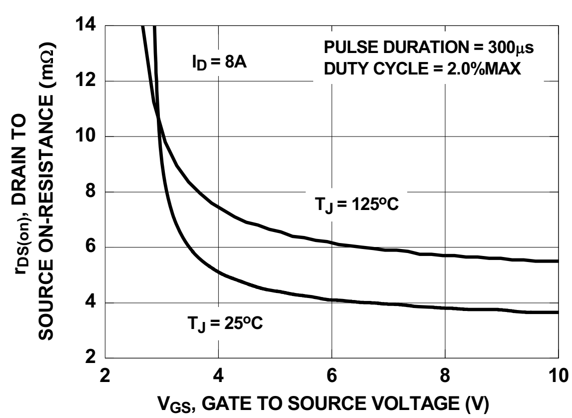


Figure 15. On-Resistance vs Gate to Source Voltage

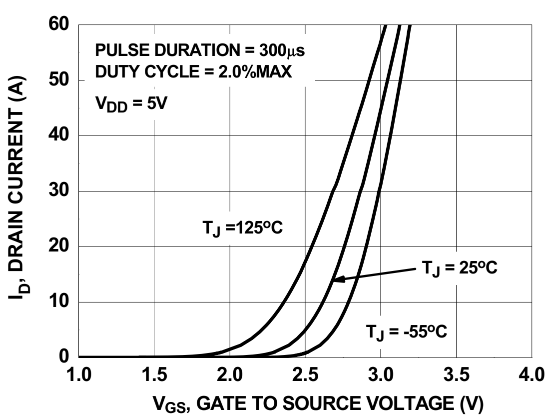


Figure 16. Transfer Characteristics

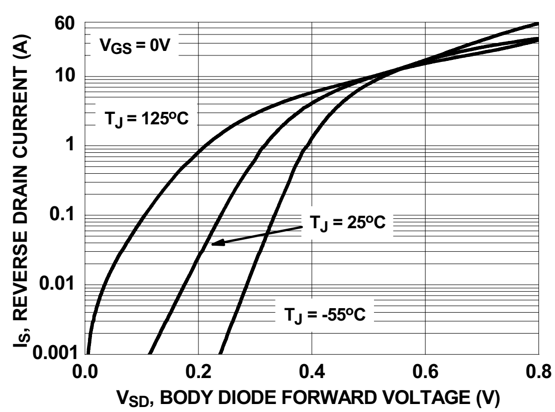


Figure 17. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics

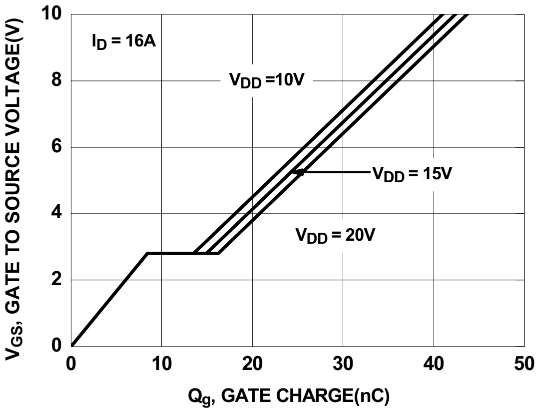


Figure 18. Gate Charge Characteristics

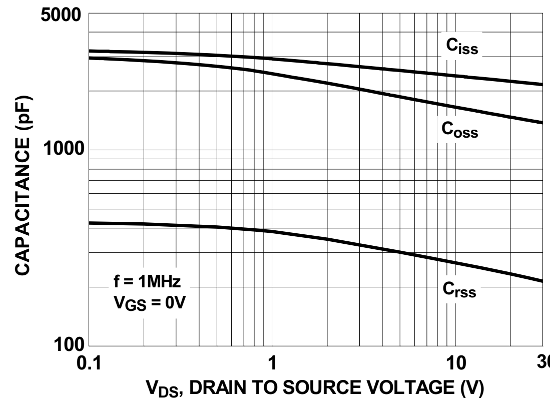
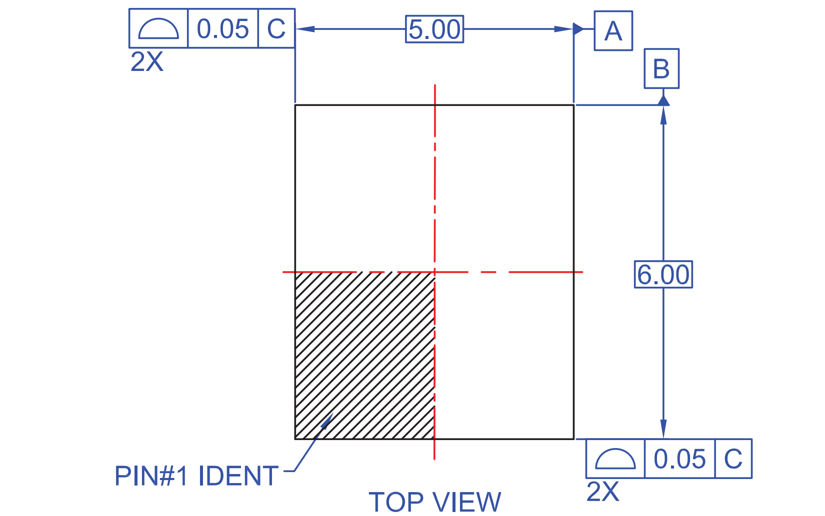
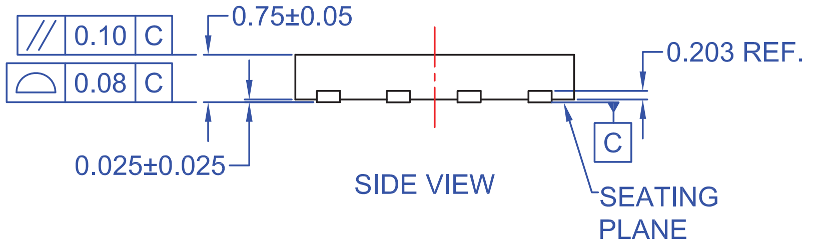


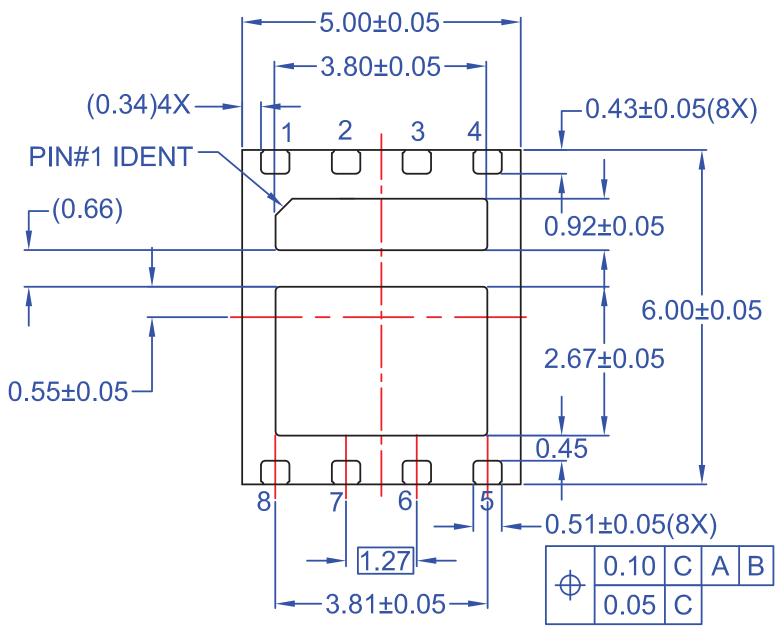
Figure 19. Capacitance vs Drain to Source Voltage



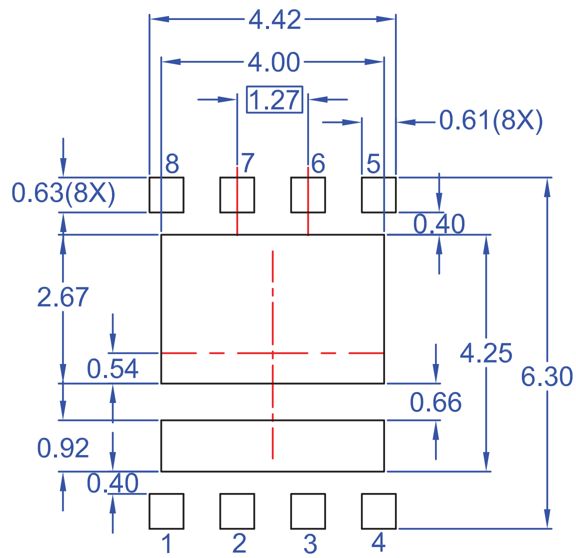
TOP VIEW



SIDE VIEW



BOTTOM VIEW



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Definition of Terms

Datasheet Identification	Product Status	Definition
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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