FAIRCHILD SEMICONDUCTOR®

December 2010

# FDN86246

## N-Channel PowerTrench® MOSFET

### 150 V, 1.6 A, 261 mΩ

## Features

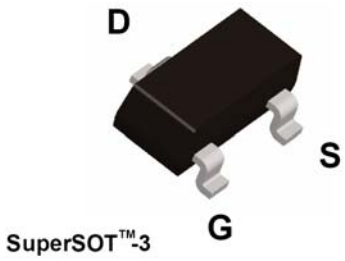
- Max $r_{DS(on)}$ = 261 mΩ at $V_{GS}$ = 10 V, $I_D$ = 1.6 A
- Max $r_{DS(on)}$ = 359 mΩ at $V_{GS}$ = 6 V, $I_D$ = 1.4 A
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handling capability in a widely used surface mount package
- Fast switching speed
- 100% UIL tested
- RoHS Compliant

## General Description

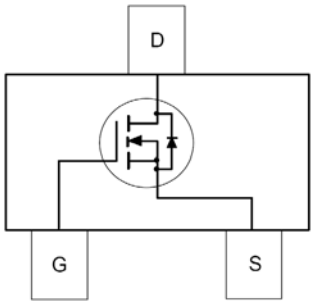
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been optimized for $r_{DS(on)}$, switching performance and ruggedness.

## Application

- PD Switch




SuperSOT™-3




## MOSFET Maximum Ratings $T_A$ = 25 °C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | 150 | V |
| $V_{GS}$ | Gate to Source Voltage | | ±20 | V |
| $I_D$ | -Continuous | (Note 1a) | 1.6 | A |
| | -Pulsed | | 6 | |
| $E_{AS}$ | Single Pulse Avalanche Energy | (Note 3) | 13 | mJ |
| $P_D$ | Power Dissipation | (Note 1a) | 1.5 | W |
| | Power Dissipation | (Note 1b) | 0.6 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | -55 to +150 | °C |

### Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | (Note 1) | 75 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | (Note 1a) | 80 | |

### Package Marking and Ordering Information

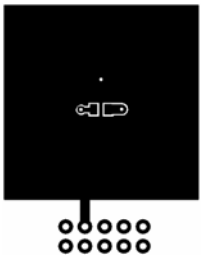
| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| 246 | FDN86246 | SSOT-3 | 7 ” | 8 mm | 3000 units |

## Electrical Characteristics $T_J$ = 25 °C unless otherwise noted

| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = 250 μA, $V_{GS}$ = 0 V | 150 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C | | 106 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 120 V, $V_{GS}$ = 0 V | | | 1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±20 V, $V_{DS}$ = 0 V | | | ±100 | nA |
| **On Characteristics (Note 2)** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | 2 | 3.4 | 4 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = 250 μA, referenced to 25 °C | | -9 | | mV/°C |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = 10 V, $I_D$ = 1.6 A | | 195 | 261 | mΩ |
| | | $V_{GS}$ = 6 V, $I_D$ = 1.4 A | | 242 | 359 | |
| | | $V_{GS}$ = 10 V, $I_D$ = 1.6 A, $T_J$ = 125 °C | | 359 | 481 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 1.6 A | | 4 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 75 V, $V_{GS}$ = 0 V, f = 1 MHz | | 168 | 225 | pF |
| $C_{oss}$ | Output Capacitance | | | 21 | 30 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 1.6 | 5 | pF |
| $R_g$ | Gate Resistance | | | 0.9 | | Ω |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = 75 V, $I_D$ = 1.6 A, $V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | 4.5 | 10 | ns |
| $t_r$ | Rise Time | | | 1.1 | 10 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 8 | 16 | ns |
| $t_f$ | Fall Time | | | 2.9 | 10 | ns |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V to 10 V; $V_{DD}$ = 75 V, $I_D$ = 1.6 A | | 2.9 | 5 | nC |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = 0 V to 5 V; $V_{DD}$ = 75 V, $I_D$ = 1.6 A | | 1.6 | 3 | nC |
| $Q_{gs}$ | Gate to Source Gate Charge | $V_{DD}$ = 75 V, $I_D$ = 1.6 A | | 0.9 | | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | $V_{DD}$ = 75 V, $I_D$ = 1.6 A | | 0.8 | | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 1.6 A (Note 2) | | 0.83 | 1.3 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 1.6 A, di/dt = 100 A/μs | | 44 | 70 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | | 29 | 47 | nC |

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 80 °C/W when mounted on a 1 $in^2$ pad of 2 oz copper

b) 180 °C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

3. Starting $T_J$ = 25 °C; N-ch: L = 3 mH, $I_{AS}$ = 3 A, $V_{DD}$ = 150 V, $V_{GS}$ = 10 V.

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

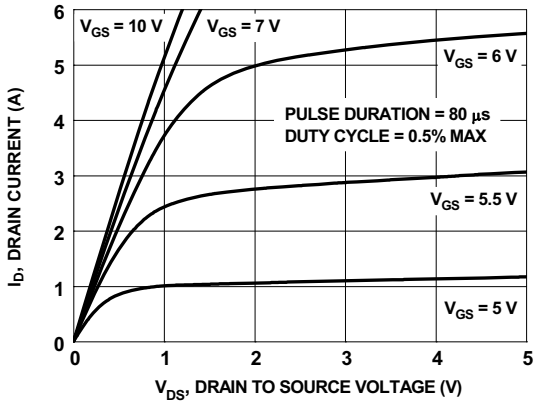



**Figure 1. On-Region Characteristics**

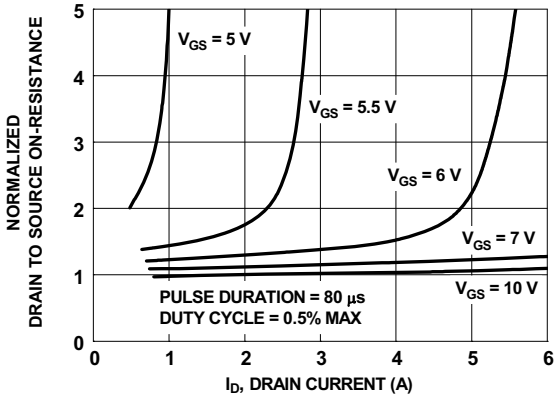



**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**

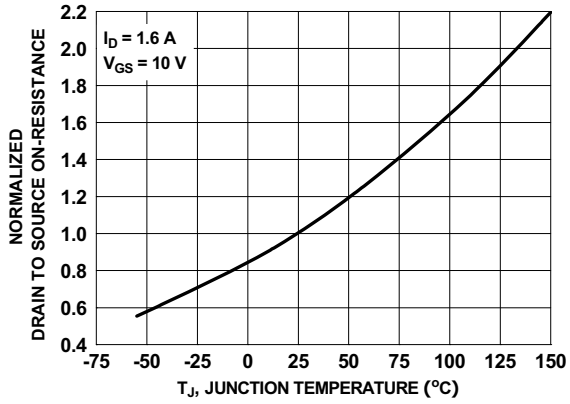



**Figure 3. Normalized On-Resistance vs Junction Temperature**

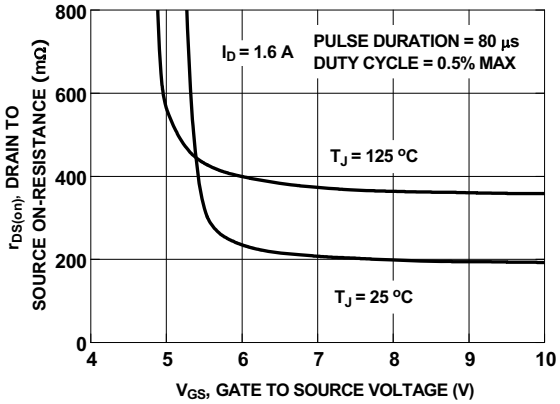



**Figure 4. On-Resistance vs Gate to Source Voltage**

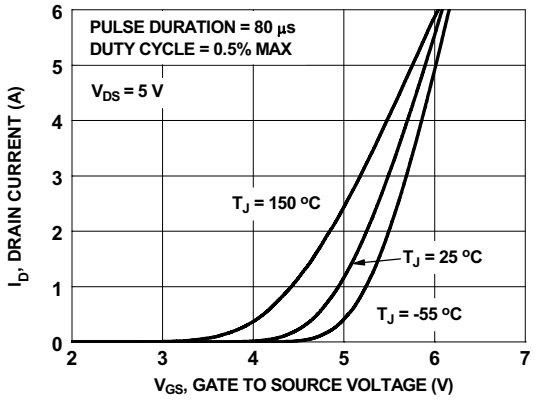



**Figure 5. Transfer Characteristics**

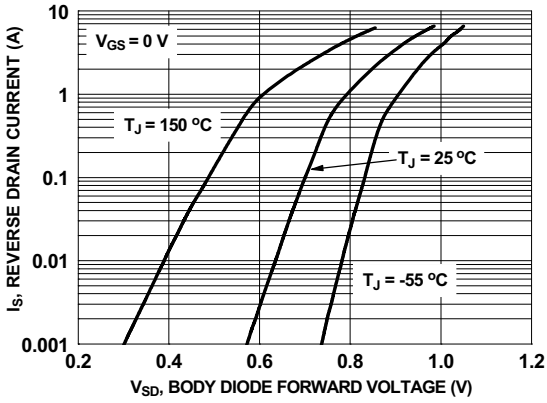



**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

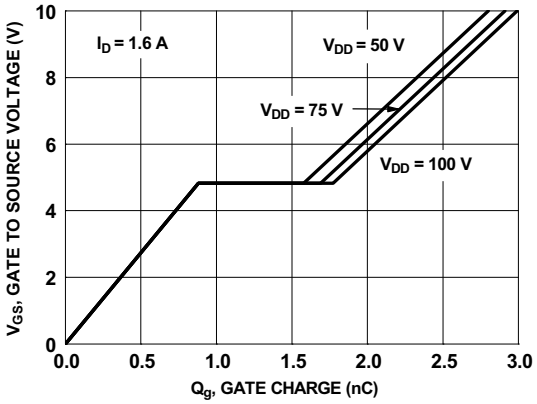



**Figure 7. Gate Charge Characteristics**

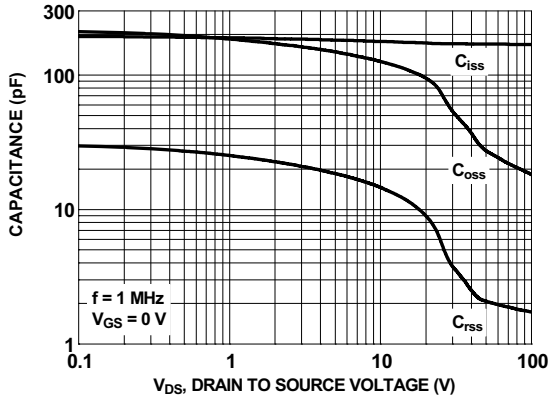



**Figure 8. Capacitance vs Drain to Source Voltage**

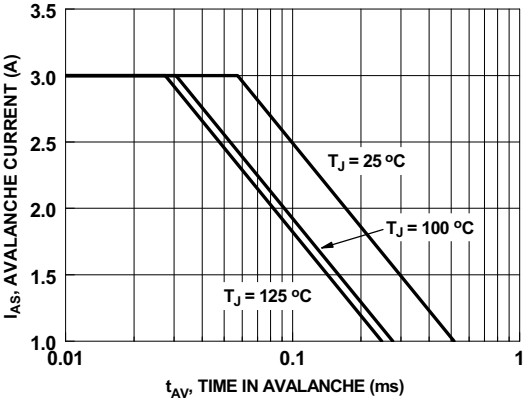



**Figure 9. Unclamped Inductive Switching Capability**

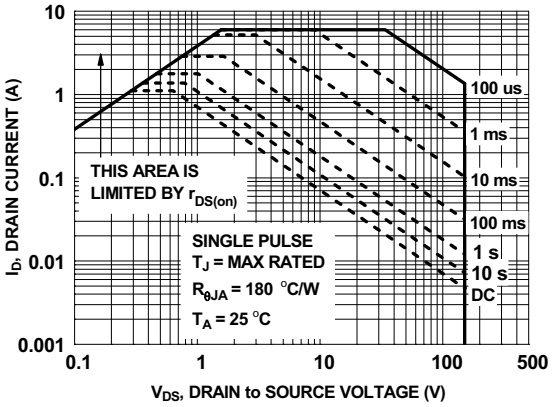



**Figure 10. Forward Bias Safe Operating Area**

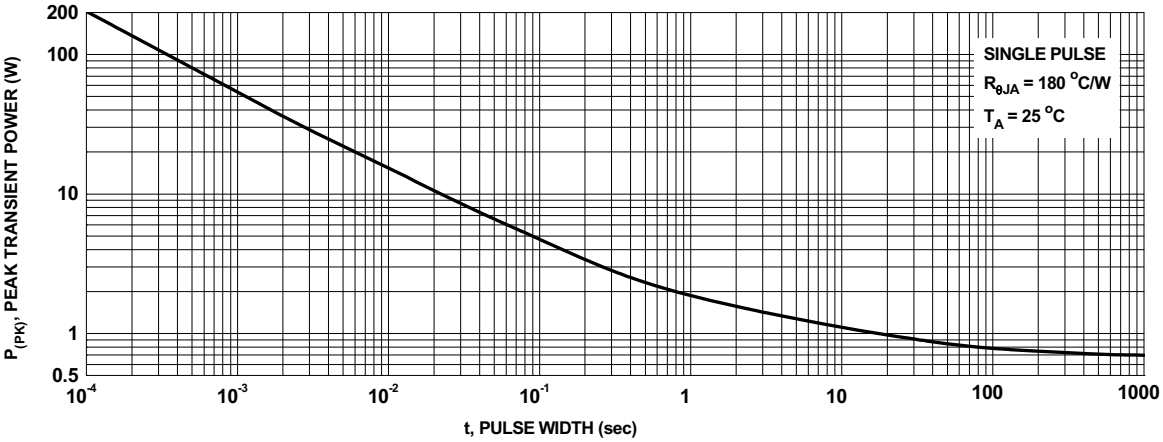



**Figure 11. Single Pulse Maximum Power Dissipation**

## Typical Characteristics $T_J$ = 25 °C unless otherwise noted

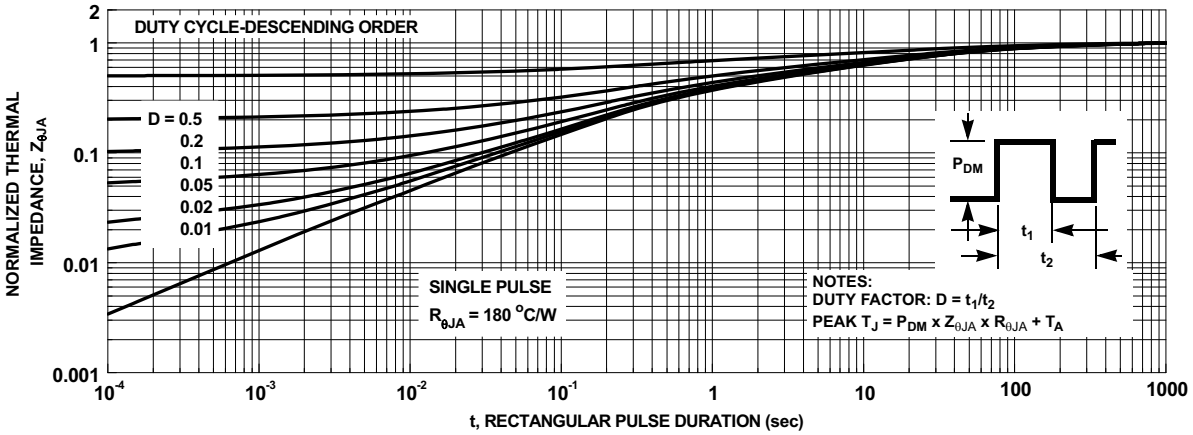



**Figure 12. Junction-to-Ambient Transient Thermal Response Curve**

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