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October 2011

FMS6404
Precision Composite Video Output with Sound Trap and Group Delay Compensation

Features

- 7.6MHz 5th-Order Composite Video Filter
- 14dB Notch at 4.425MHz to 4.6MHz for Sound Trap Capable of Handling Stereo
- 50dB Stopband Attenuation at 27MHz on CV Output
- > 0.5dB Flatness to 4.2MHz on CV Output
- Equalizer and Notch Filter for Driving RF Modulator with Group Delay of -180ns
- No External Frequency Selection Components or Clocks
- < 5ns Group Delay on CV Output
- AC-Coupled Input
- AC- or DC-Coupled Output
- Capable of PAL Frequency for CV
- Continuous Time Low-Pass Filters
- <1.4% Differential Gain with 0.7° Differential Phase on CV Channel
- Integrated DC Restore Circuitry with Low Tilt

Applications

- Cable Set-Top Boxes
- Satellite Set-Top Boxes
- DVD Players

Description

The FMS6404 is a single composite video 5th-order Butterworth low-pass video filter optimized for minimum overshoot and flat group delay. The device contains an audio trap that removes video information in a spectral location of the subsequent RF audio carrier. The group delay compensation circuit pre-distorts the signal to compensate for the inherent receiver intermediate frequency (IF) filter's group delay distortion.

In a typical application, the composite video from the DAC is AC coupled into the filter. The CV input has DC-restore circuitry to clamp the DC input levels during video synchronization. The clamp pulse is derived from the CV channel.

All outputs are capable of driving $2V_{PP}$, AC- or DC-coupled, into either a single or dual video load. A single video load consists of a series 75Ω impedance matching resistor connected to a terminated 75Ω line. This presents a total of 150Ω of loading to the part. A dual load would be two of these in parallel, which presents a total of 75Ω to the part. The gain of the CV signal is 6dB with $1V_{PP}$ input levels. All video channels are clamped during synchronization to establish the appropriate output voltage reference levels.

Related Resources

- *AN-6024 – FMS6xxx Product Series Understanding Analog Video Signal Clamps, Bias, DC Restore, and AC or DC coupling Methods*
- *AN-6041 – PCB Layout Considerations for Video Filter / Drivers*

Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FMS6404CSX	-40°C to +70°C	8-Lead, Small-Outline Integrated Circuit (SOIC), JEDEC MS-012, .150" Narrow Body	2500 Units per Reel

Block Diagram

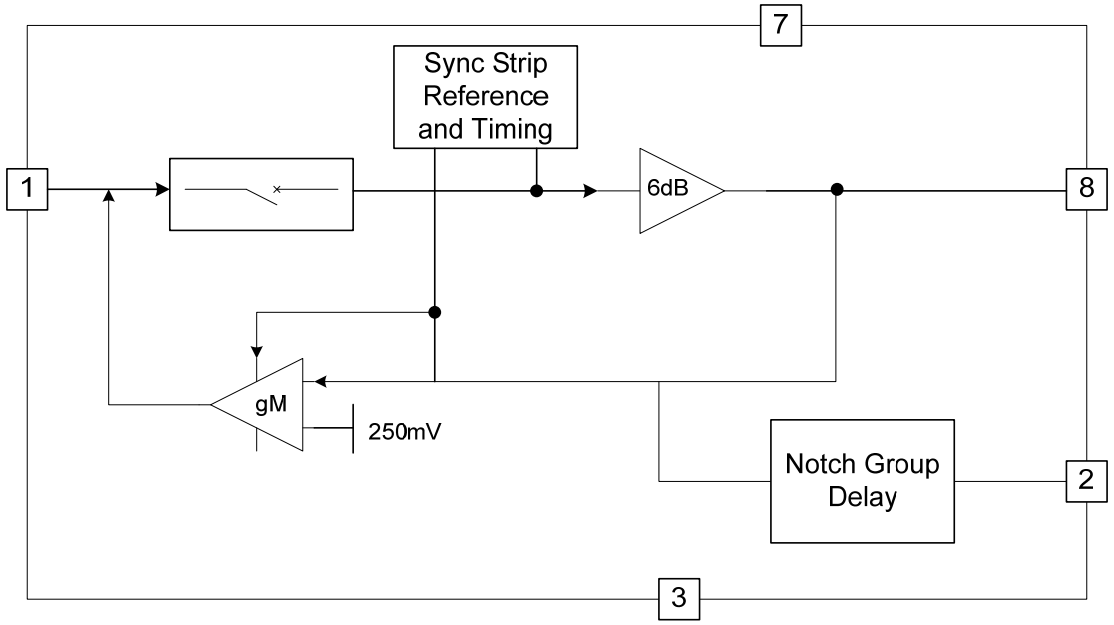

Figure 1. Block Diagram

Pin Configuration

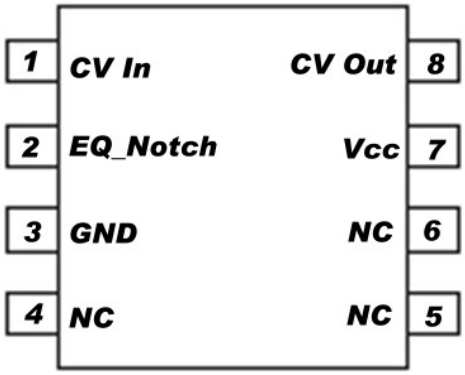

Figure 2. Pin Assignments (Top View)

Pin Definitions

Pin#	Name	Type	Description
1	CV In	Input	Composite video input
2	EQ_Notch	Output	Composite video output to RF modulator
3	GND	Power	Device ground connection
4	NC	NA	No connection
5	NC	NA	No connection
6	NC	NA	No connection
7	Vcc	Power	Device power connection
8	CV Out	Output	Composite video output

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	DC Supply Voltage	-0.3	6.0	V
V_{IO}	Analog and Digital I/O	-0.3	V_{CC}+0.3	V
V_{OUT}	Maximum Output Current, Do Not Exceed		100	mA

Electrostatic Discharge Information

Symbol	Parameter	Min.	Unit
ESD	Human Body Model, JESD22-A114	8	kV
	Charged Device Model, JESD22-C101	2	

Reliability Information

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_J	Junction Temperature			+150	°C
T_{STG}	Storage Temperature Range	-65		+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)			+300	°C
□$_{JA}$	Thermal Resistance, JEDEC Standard, Multilayer Test Board, Still Air		90		°C/W

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_A	Operating Temperature Range	0		+70	°C
V_{CC}	Supply Voltage Range	4.75	5.00	5.25	V

DC Electrical Characteristics

T_A=25°C, V_{CC}=5.0V, R_S=37.5Ω, all inputs are AC-coupled with 0.1μF, and all outputs are AC coupled with 220μF into 150Ω load; unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage Range	V_S Range	4.75	5.00	5.25	V
I_{CC}	Quiescent Supply Current	V_S=+5.0V, No Load	50	70	90	mA
V_{IN}	Video Input Voltage Range	Referenced to GND if DC Coupled		1.4		V_{PP}
PSRR	Power Supply Rejection Ratio	DC		-50		dB
I_{SC}	Output Short Circuit Current	CV, EQ_NOTCH to GND		85		mA

AC Electrical Characteristics

T_A=25°C, V_{CC}=5.0V, R_S=37.5Ω, all inputs are AC-coupled with 0.1µF, and all outputs are AC coupled with 220µF into 150Ω load, unless otherwise noted.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
AV_{CV}	Low Frequency Gain CV_{OUT}	at 400kHz	5.8	6.0	6.2	dB
AV_{EQ}	Low Frequency Gain (EQ_NOTCH)	at 400kHz	5.7	6.0	6.4	dB
CV_{sync}	CV_{OUT} Output Level (During Sync)	Sync Present on CV_{IN} (After 6dB Gain)		0.35	0.50	V
EQ_{sync}	EQ_NOTCH Output Level (During Sync)	Sync Present on CV_{IN} (After 6dB Gain)		0.35	0.50	V
t_{CLAMP}	Clamp Response Time CV_{OUT}	Settled to within 10mV		5		ms
f_{FLAT}	Gain Flatness to 4.2MHz CV_{OUT}		-0.5	0	0.5	dB
f_C	-3dB Bandwidth	CV_{OUT} Channel	6.7	7.6		MHz
f_{SB}	Stopband Attenuation CV_{OUT}	at 27MHz	40	50		dB
dG	Differential Gain	CV_{OUT}		1.4	3.0	%
dq	Differential Phase	CV_{OUT}		0.7	1.5	°
THD	Output Distortion	V_{OUT}=1.4V_{pp} at 3.58MHz		0.3		%
X_{TALK}	Crosstalk	V_{OUT}=1.4V_{pp} at 3.58MHz		-50		dB
SNR	SNR CV_{OUT} Channel	NTC-7 Weighting 4.2MHz Low-Pass V_{IN}=714mV, V_{OUT}=1.428V_{PP}/1.010Vrms	70	75		dB
	SNR EQ_NOTCH Channel	NTC-7 Weighting 4.2MHz Low-Pass V_{IN} =714mV V_{OUT}=1.428Vpp/1.010Vrms	65	70		dB
t_{pd}	Propagation Delay	at 400kHz		112		ns
GD	Group Delay CV_{OUT}	at 3.58MHz (Reference to 400KHz)	-5	0	5	ns
t_{CLGCV}	Chroma-Luma Gain CV_{OUT}	f=3.58MHz (Reference to 400kHz)	98	100	102	%
t_{CLDCV}	Chroma-Luma Delay CV_{OUT}	f=3.58MHz (Reference to 400kHz)	-10	0	10	ns
t_{GDEQ}	Group Delay EQ_NOTCH	f=3.58MHz (Reference to 400kHz)	-195	-180	-165	ns
t_{CLGEQ}	Chroma-Luma Gain EQ_NOTCH	f=3.58MHz (Reference to 400kHz)	95	100	105	%
t_{CLDEQ}	Chroma-Luma Delay EQ_NOTCH	f=3.58MHz (Reference to 400kHz)	-195	-180	-165	ns
dG_{EQ}	Differential Gain	EQ_NOTCH Channel		0.3	1.0	%
dq_{EQ}	Differential Phase	EQ_NOTCH Channel		0.30	0.75	%
MCF	Modulator Channel Flatness	EQ_NOTCH from 400kHz to 3.75MHz	-0.5	0	0.5	dB
AV_{PK}	Gain Peaking	EQ_NOTCH from >3.75MHz to 4.2MHz	-0.5	0	0.5	dB
Atten1	Notch Attenuation 1	EQ_NOTCH at 4.425MHz	14			dB
Atten2	Notch Attenuation 2	EQ_NOTCH at 4.5MHz	20			dB
Atten3	Notch Attenuation 3	EQ_NOTCH at 4.6MHz	14			dB
t_{PASS}	Passband Group Delay EQ_NOTCH	f=400kHz to f=3MHz	-35		35	ns

Typical Performance Characteristics

Unless otherwise noted, T_A = 25°C, V_{CC} = 5.0V, R_s = 37.5Ω, and AC-coupled output into 150Ω load, CV_{OUT}.

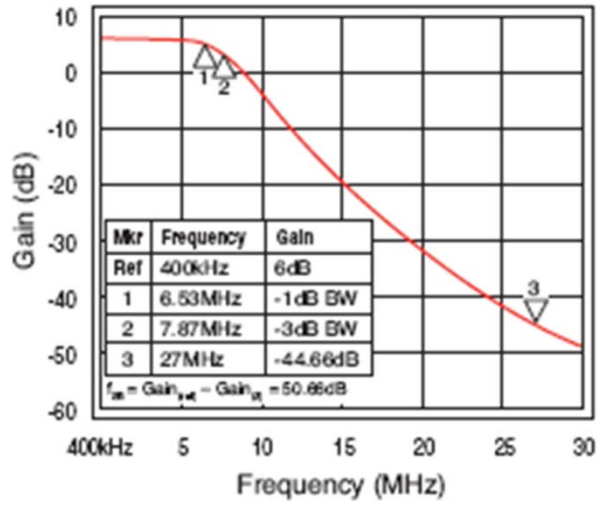

Figure 3. Frequency Response

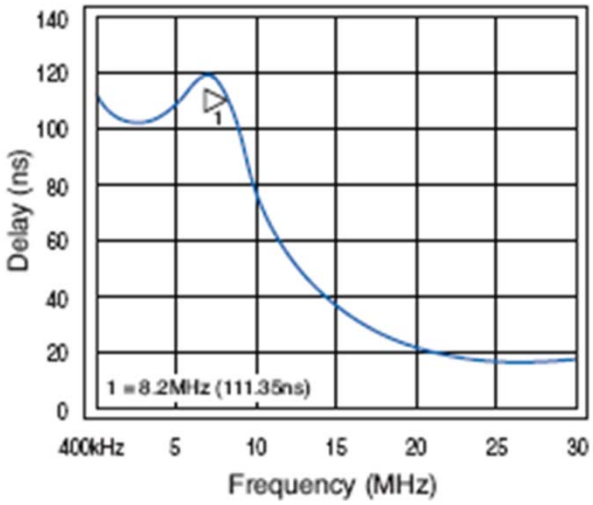

Figure 4. Group Delay vs. Frequency

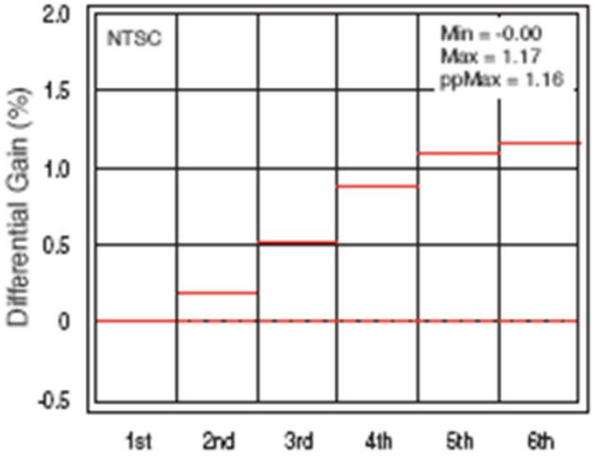

Figure 5. Differential Gain

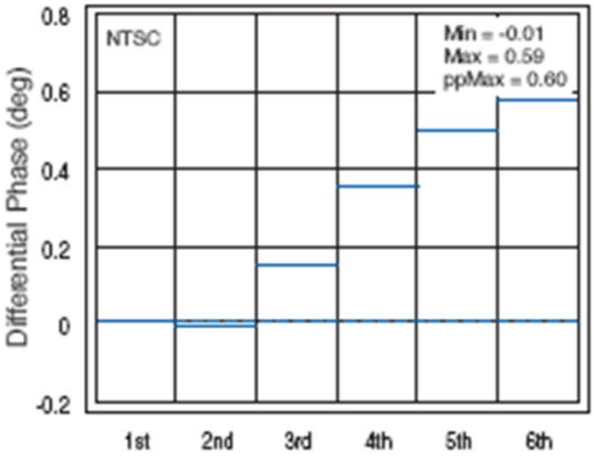

Figure 6. Differential Phase

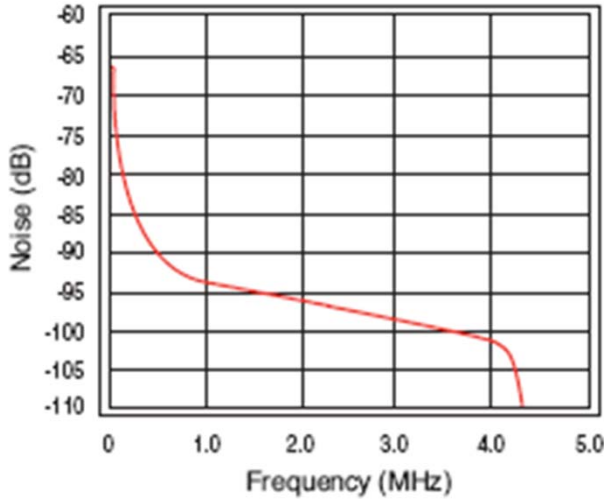

Figure 7. Noise vs. Frequency

Typical Performance Characteristics

Unless otherwise noted, T_A = 25°C, V_{CC} = 5.0V, R_s = 37.5Ω, and AC-coupled output into 150Ω load, CV_{OUT}.

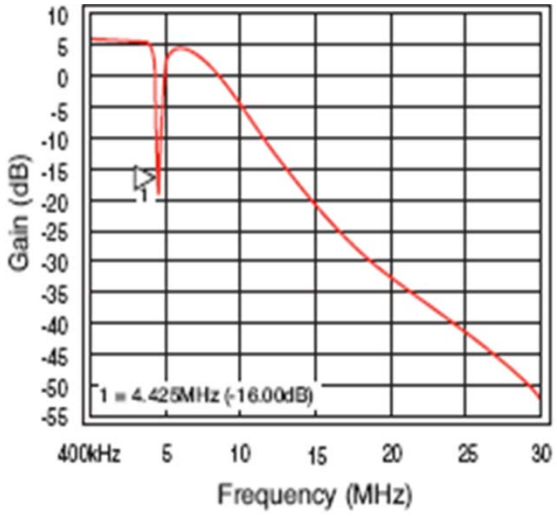

Figure 8. Modulator vs. Frequency Response

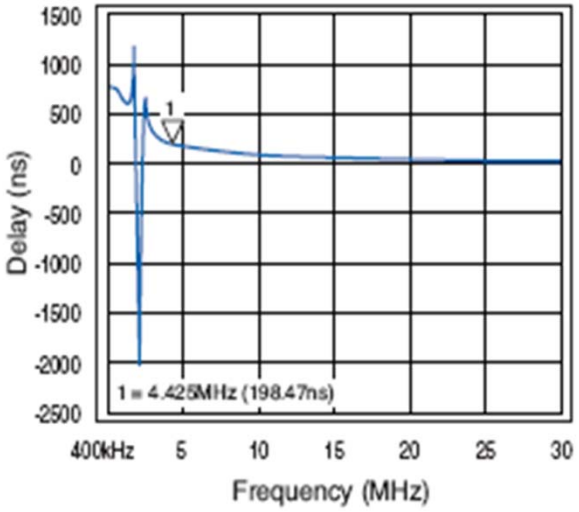

Figure 9. Delay Modulator Output

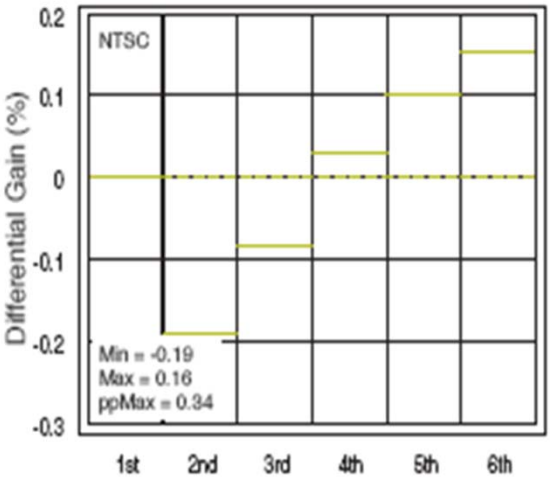

Figure 10. Differential Gain, MOD_{OUT}

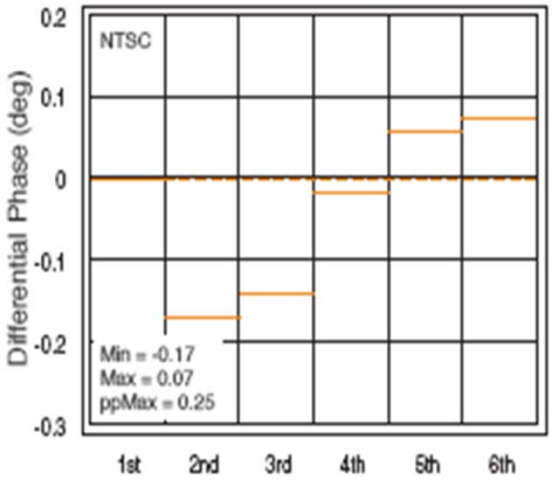

Figure 11. Differential Phase, MOD_{OUT}

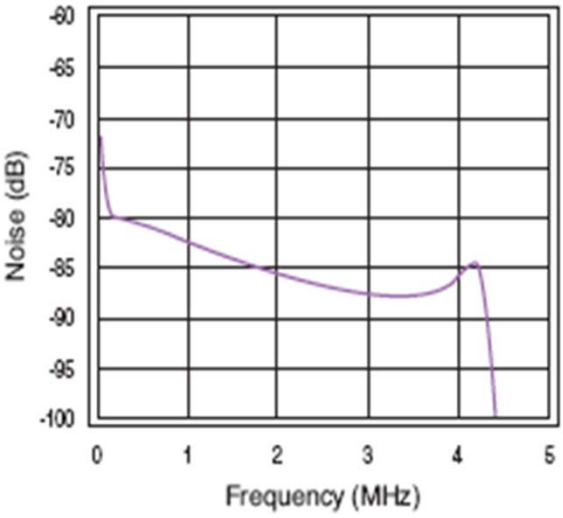

Figure 12. Noise vs. Frequency Modulator Channel

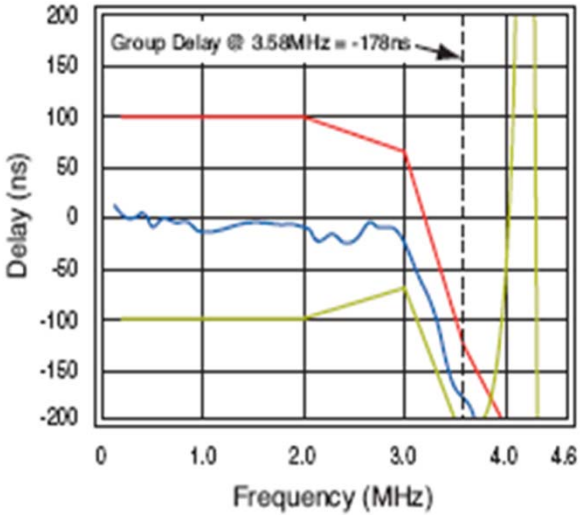

Figure 13. Group Delay vs. Frequency

Applications Information

Layout Considerations

General layout and supply bypassing play a major role in high-frequency performance and thermal characteristics. Fairchild offers a four-layer board with full power and ground planes board to guide layout and aid device evaluation. Following this layout configuration provides optimum performance and thermal characteristics for the device. For best results, follow the steps and recommended routing rules below.

Recommended Routing / Layout Rules

- Do not run analog and digital signals in parallel.
- Use separate analog and digital power planes to supply power.
- Traces must run on top of the ground plane.
- No trace should run over ground/power splits.
- Avoid routing at 90-degree angles.
- Minimize clock and video data trace length differences.
- Include 10µF and 0.1µF ceramic power supply bypass capacitors.
- Place the 0.1µF capacitor within 2.54mm (0.1in) of the device power pin.
- Place the 10µF capacitor within 19.05mm (0.75in) of the device power pin.
- For multi-layer boards, use a large ground plane to help dissipate heat.
- For two-layer boards, use a ground plane that extends beyond the device body at least 12.7mm (0.5in) on all sides. Include a metal paddle under the device on the top layer.
- Minimize all trace lengths to reduce series inductance.

Output Considerations

The outputs are DC offset from the input by 150mV; therefore, V_{OUT} = 2 • V_{IN} DC + 150mV. This offset is required for optimal performance from the output driver and is held at the minimum value to decrease the standing DC current into the load. Since the FMS6404 has a 2 x (6dB) gain, the output is typically connected via a 75Ω-series back-matching resistor, followed by the 75Ω video cable. Due to the inherent divide-by-two of this configuration, the blanking level at the load of the video signal is always less than 1V. When AC-coupling the output, ensure that the coupling capacitor passes the lowest frequency content in the video signal and that line time distortion (video tilt) is kept as low as possible.

The selection of the coupling capacitor is a function of the subsequent circuit input impedance and the leakage current of the input being driven. To obtain the highest quality output video signal, the series termination resistor must be placed as close to the device output pin as possible. This greatly reduces the parasitic capacitance and inductance effect on the output driver. The distance from the device pin to the series termination resistor should be no greater than 2.54mm (0.1in).

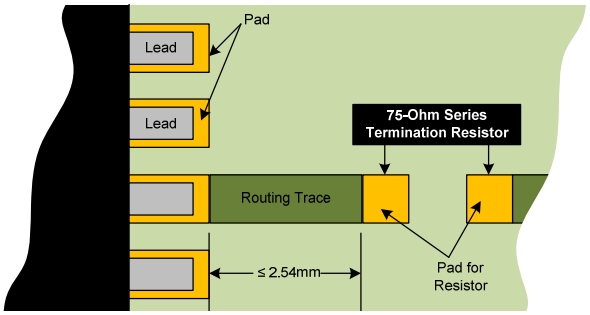

Figure 14. Termination Resistor Placement

Thermal Considerations

Since the interior of most systems, such as set-top boxes, TVs, and DVD players; is at +70ºC; consideration must be given to providing an adequate heat sink for the device package for maximum heat dissipation. When designing a system board, determine how much power each device dissipates. Ensure that devices of high power are not placed in the same location, such as directly above (top plane) or below (bottom plane) each other on the PCB.

PCB Thermal Layout Considerations

- Understand the system power requirements and environmental conditions.
- Maximize thermal performance of the PCB.
- Consider using 70µm of copper for high-power designs.
- Make the PCB as thin as possible by reducing FR4 thickness.
- Use vias in power pad to tie adjacent layers together.
- Remember that baseline temperature is a function of board area, not copper thickness.
- Modeling techniques provide a first-order approximation.

Physical Dimensions

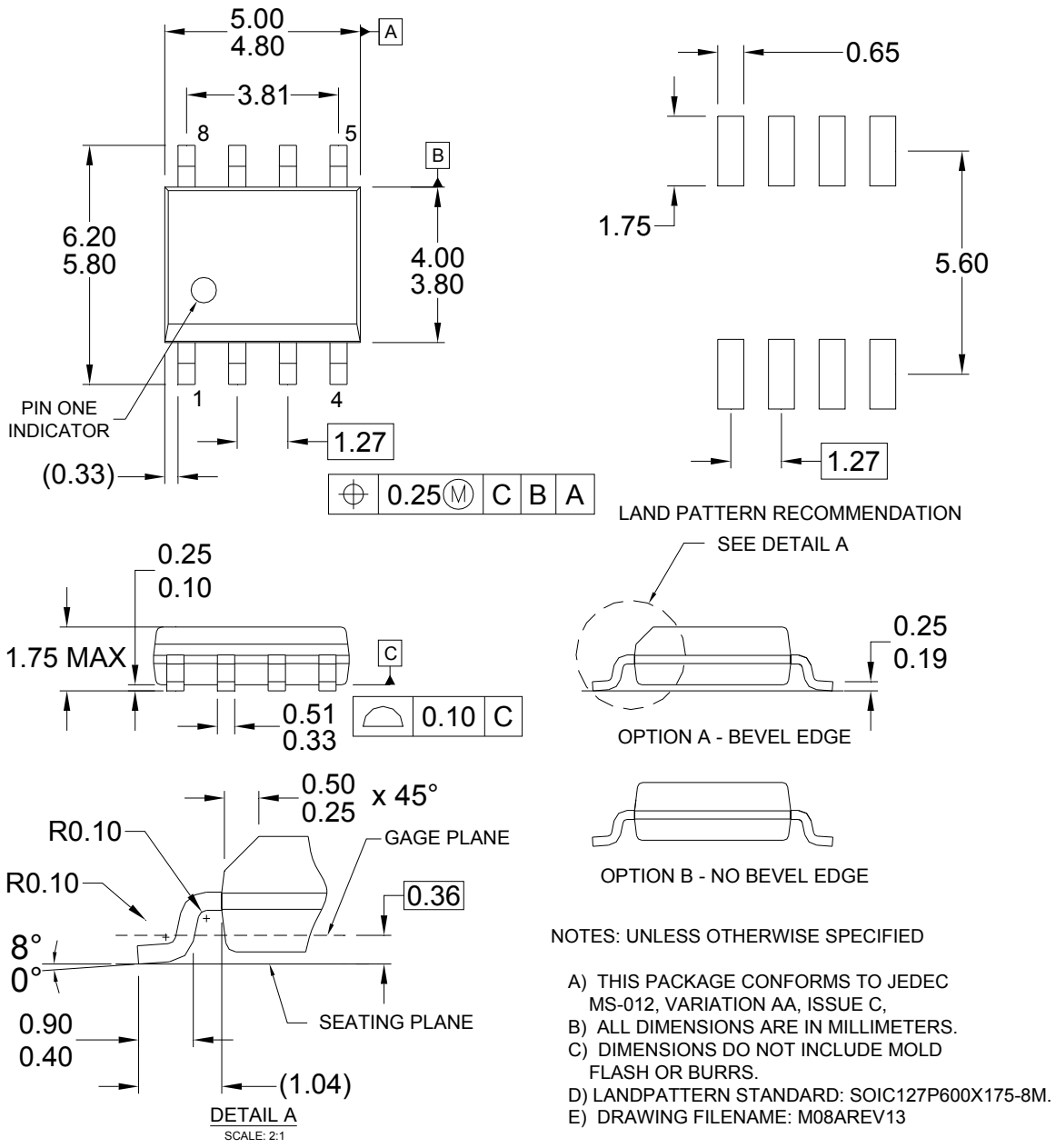

Figure 15. 8-Lead, Small-Outline Integrated Circuit (SOIC), JEDEC MS-012, .150" Narrow Body

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