May 2015

FQU5N50CTU_WS

N-Channel QFET® MOSFET

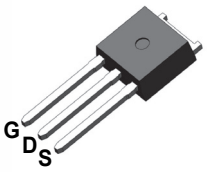
500 V, 4.0 A, 1.4 Ω

Features

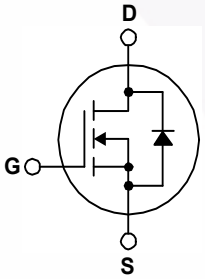
- 4.0 A, 500 V, $R_{DS(on)}$ = 1.4 Ω @V_{GS} = 10 V
- Low Gate Charge (Typ. 18 nC)
- Low Crss (Typ. 15 pF)
- Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability

Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.



I-PAK



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted.

Symbol	Parameter		FQU5N50CTU_WS	Units
V_{DSS}	Drain-Source Voltage		500	V
I_D	Drain Current - Continuous (T_C = 25°C)		4.0	A
	- Continuous (T_C = 100°C)		2.4	A
I_{DM}	Drain Current - Pulsed	(Note 1)	16	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	300	mJ
I_{AR}	Avalanche Current	(Note 1)	4	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	4.8	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Power Dissipation (T_C = 25°C)		48	W
	- Derate above 25°C		0.38	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FQU5N50CTU_WS	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	2.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	110	°C/W

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQU5N50CTU_WS	FQU5N50CS	I-PAK	Tube	N/A	N/A	75 units

Electrical Characteristics T_C = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	500	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	--	0.5	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	--	--	1	μA
		V_{DS} = 400 V, T_C = 125°C	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 2.0 A	--	1.14	1.4	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 2.0 A	--	5.2	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	480	625	pF
C_{oss}	Output Capacitance		--	80	105	pF
C_{rss}	Reverse Transfer Capacitance		--	15	20	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250 V, I_D = 5 A, V_{GS} = 10 V, R_G = 25 Ω (Note 4)	--	12	35	ns
t_r	Turn-On Rise Time		--	46	100	ns
$t_{d(off)}$	Turn-Off Delay Time		--	50	110	ns
t_f	Turn-Off Fall Time		--	48	105	ns
Q_g	Total Gate Charge	V_{DS} = 400 V, I_D = 5 A, V_{GS} = 10 V (Note 4)	--	18	24	nC
Q_{gs}	Gate-Source Charge		--	2.2	--	nC
Q_{gd}	Gate-Drain Charge		--	9.7	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	4	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	16	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 4 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 5 A, dI_F / dt = 100 A/μs (Note 4)	--	263	--	ns
Q_{rr}	Reverse Recovery Charge		--	1.9	--	μC

Notes:

1. Repetitive rating : pulse width limited by maximum junction temperature.
2. L = 21.5 mH, I_{AS} = 5 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 5 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.
4. Essentially independent of operating temperature.

Typical Characteristics

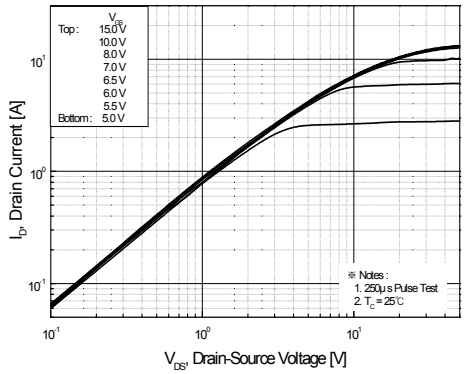


Figure 1. On-Region Characteristics

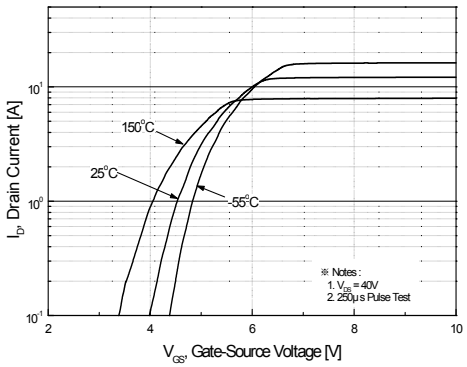


Figure 2. Transfer Characteristics

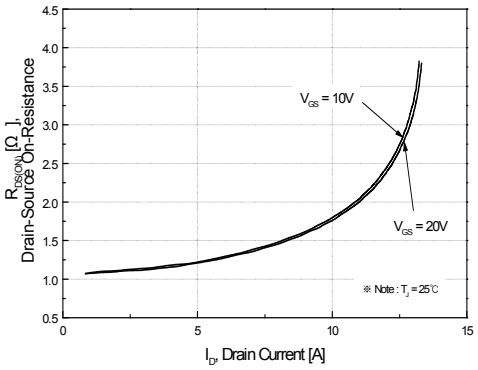


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

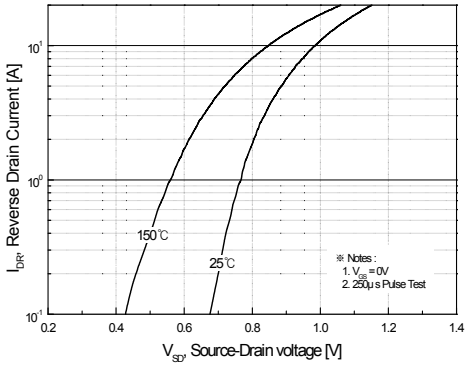


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

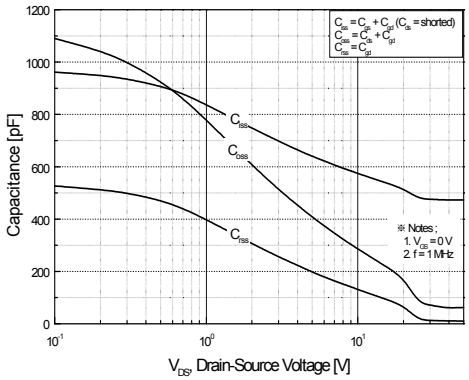


Figure 5. Capacitance Characteristics

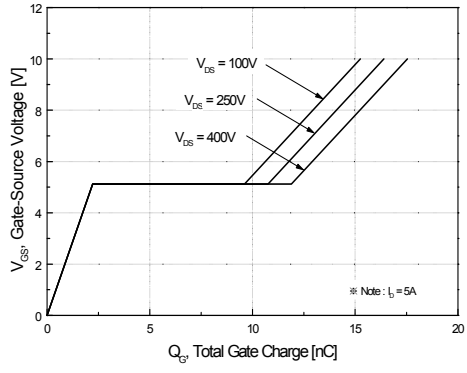


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

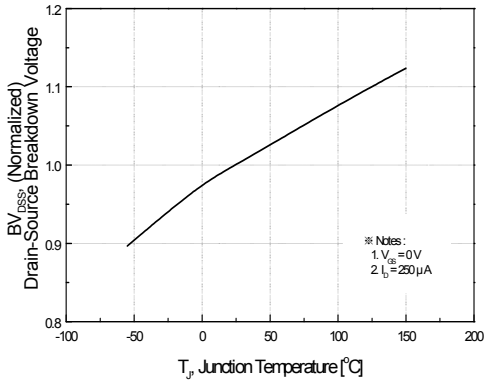


Figure 7. Breakdown Voltage Variation vs Temperature

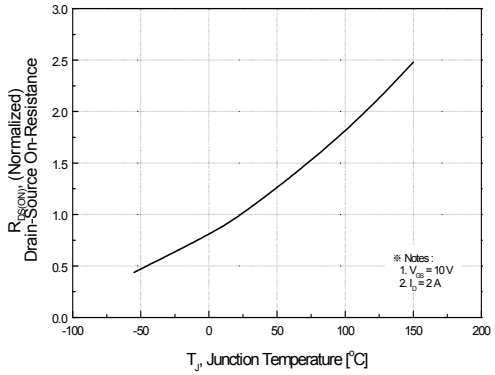


Figure 8. On-Resistance Variation vs Temperature

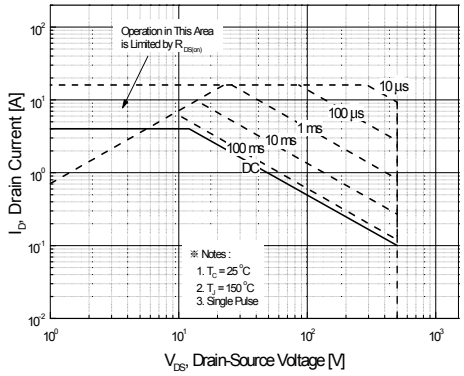


Figure 9. Maximum Safe Operating Area

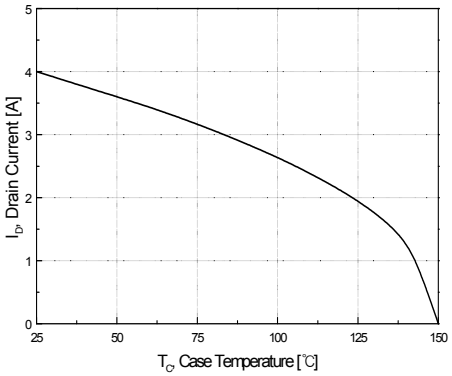


Figure 10. Maximum Drain Current vs Case Temperature

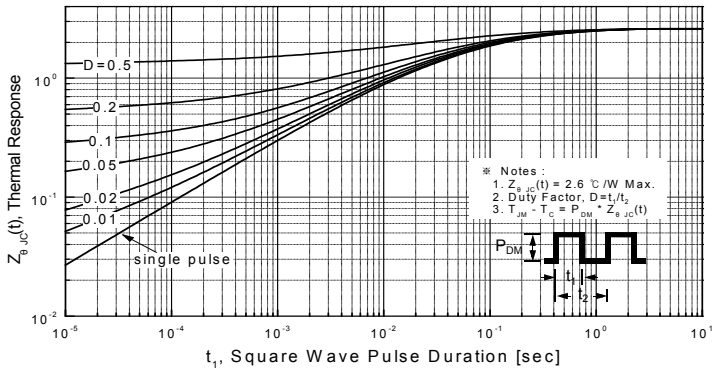


Figure 11. Transient Thermal Response Curve

Figure 12. Gate Charge Test Circuit & Waveform

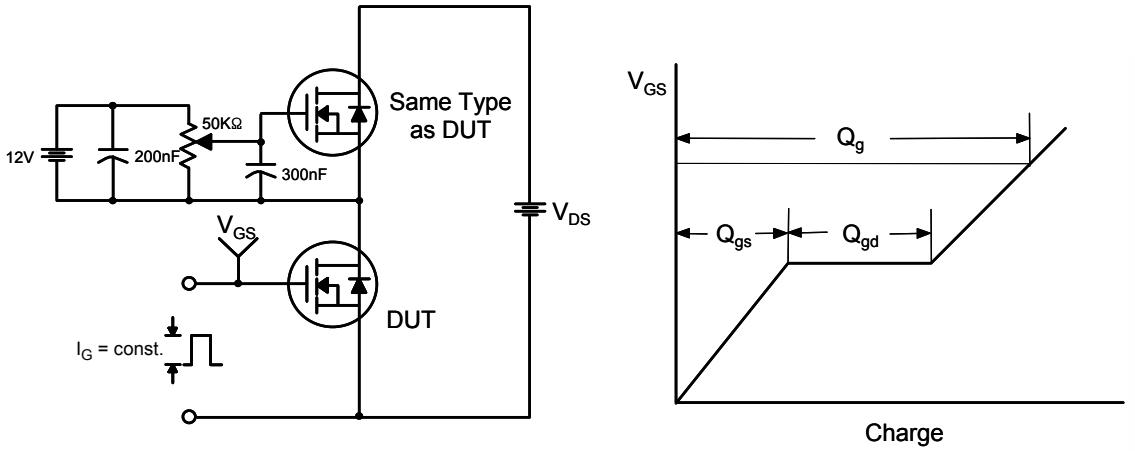


Figure 13. Resistive Switching Test Circuit & Waveforms

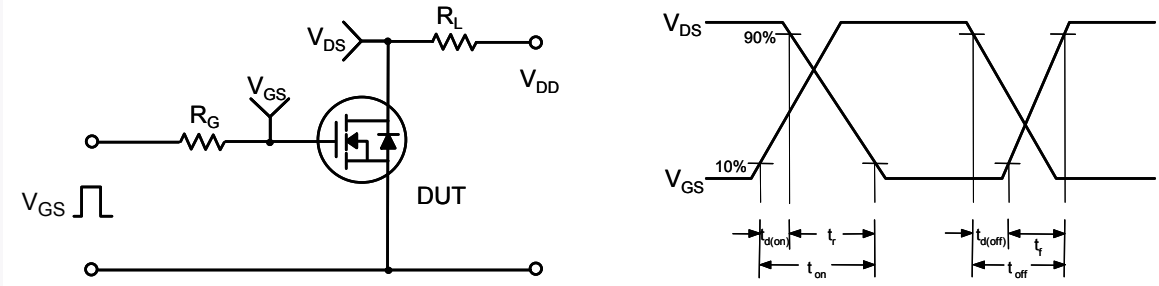


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

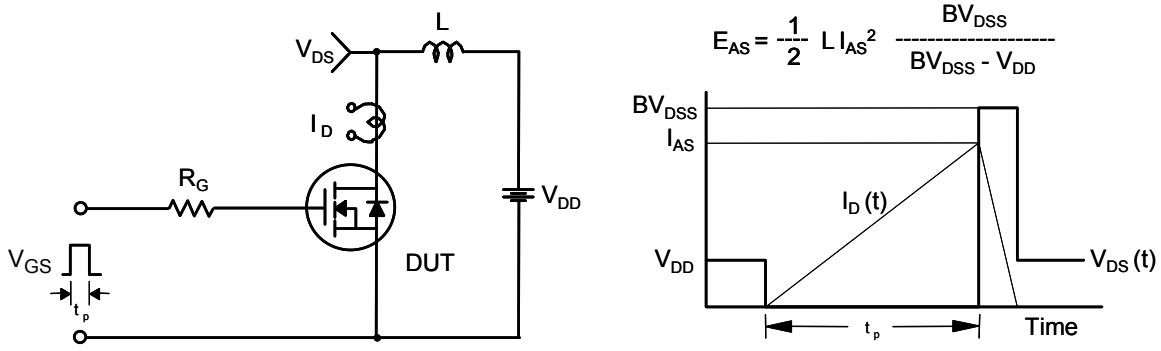
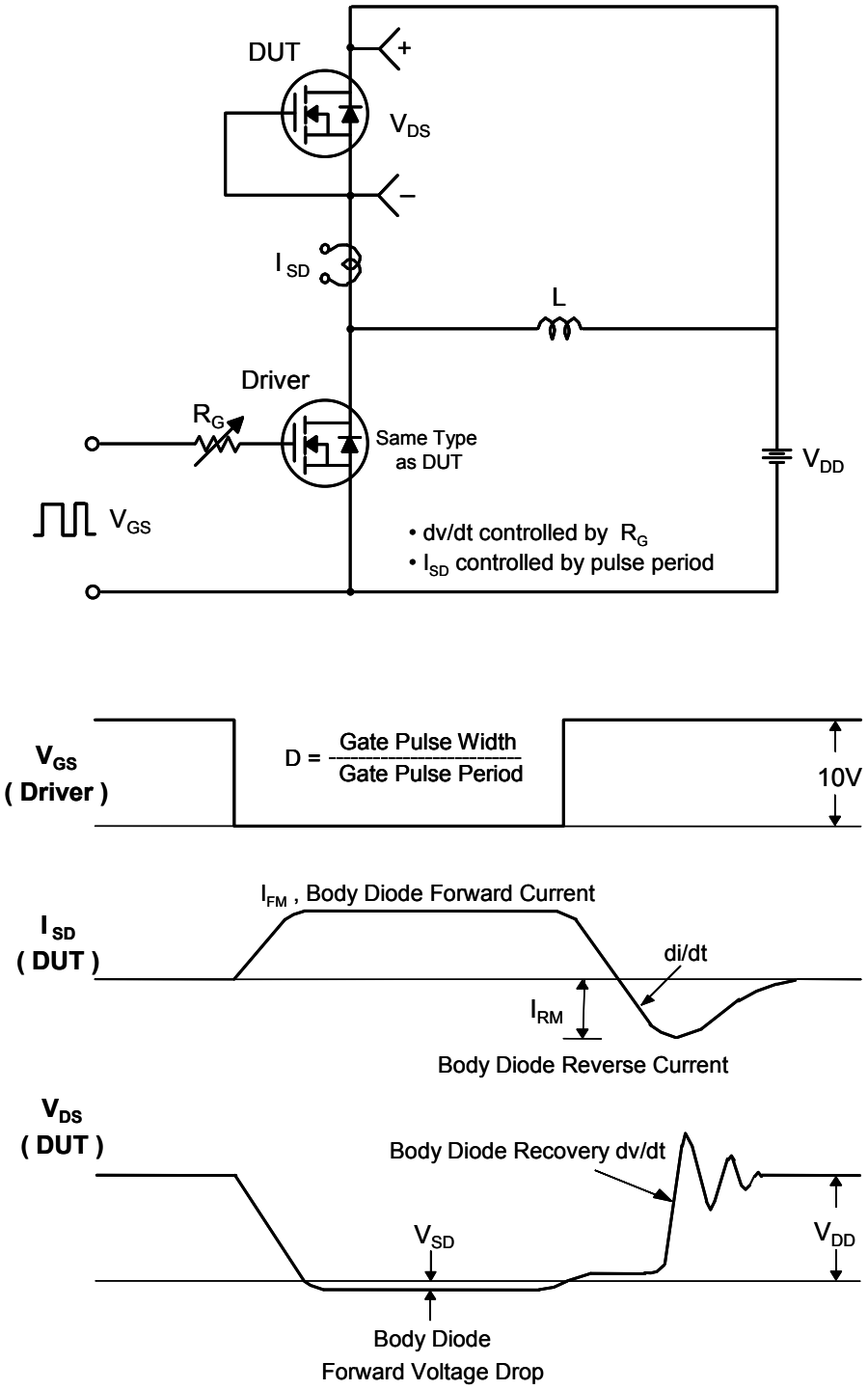
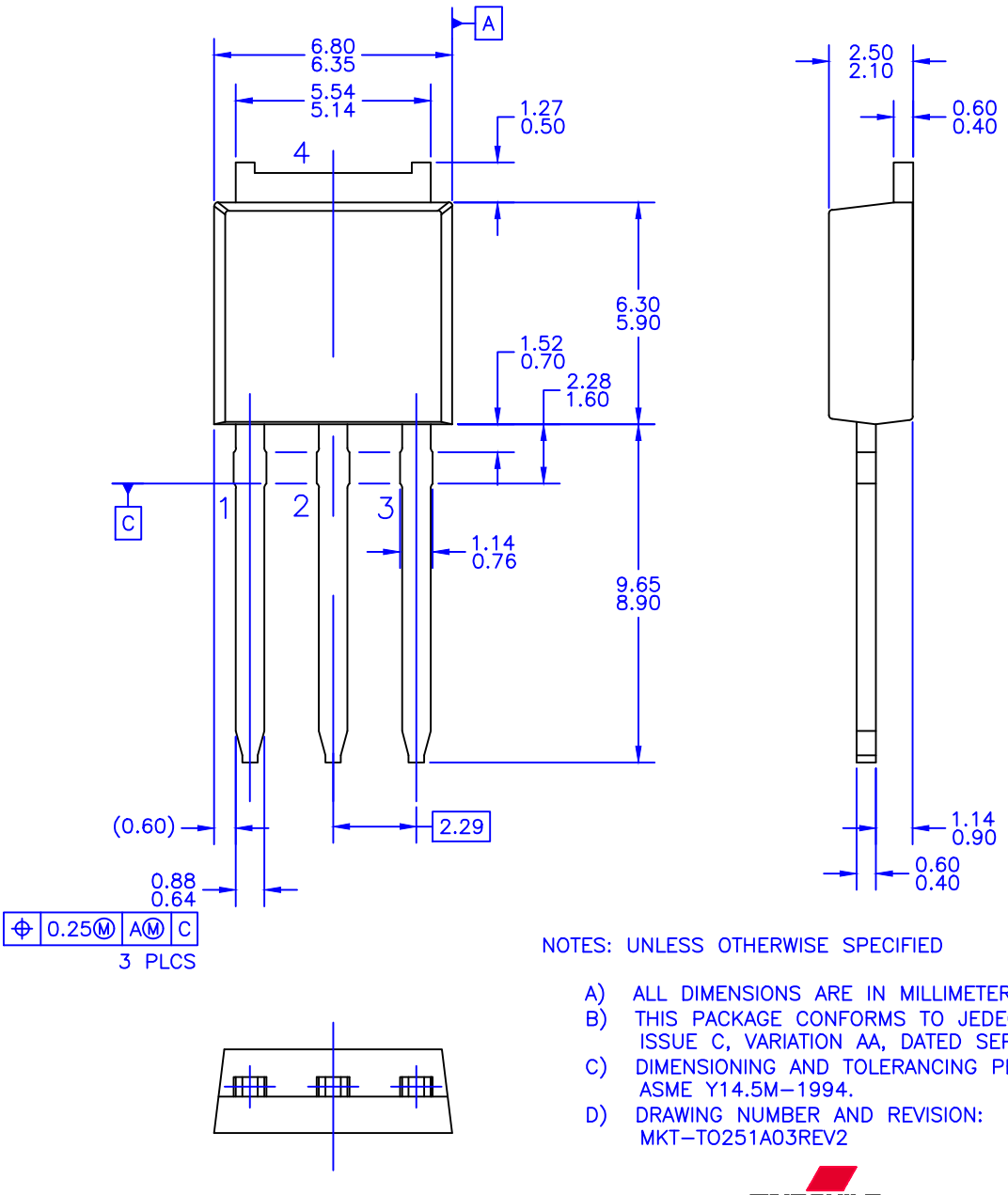


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms





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D) DRAWING NUMBER AND REVISION: MKT-TO251A03REV2

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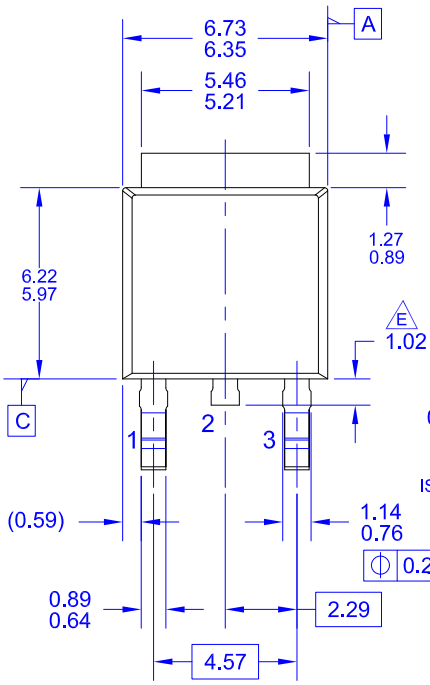
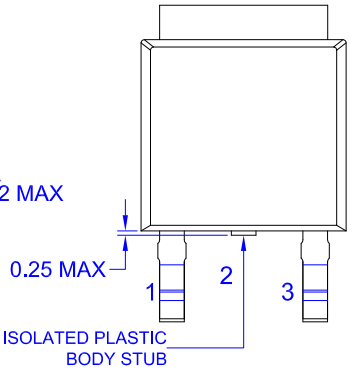
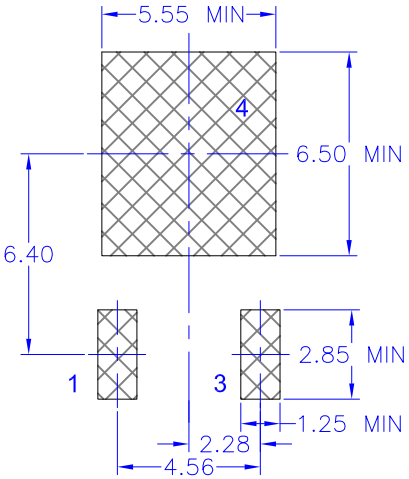


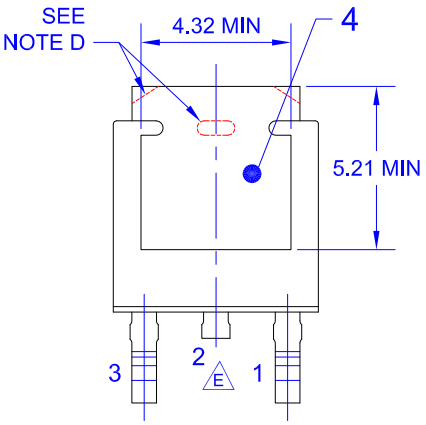
NON-DIODE PRODUCTS VERSION



DIODE PRODUCTS VERSION



LAND PATTERN RECOMMENDATION



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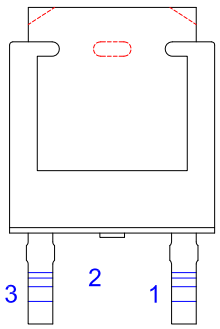
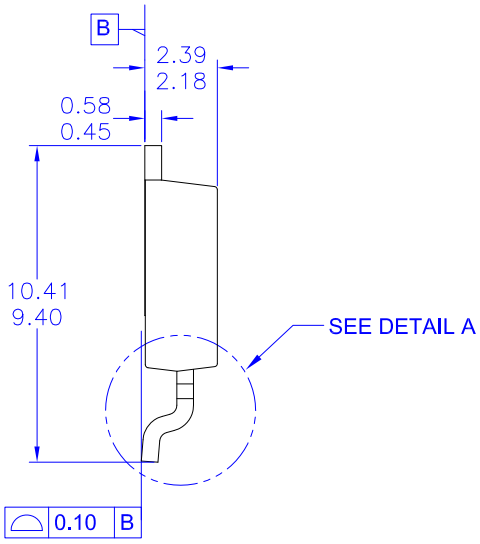


DIODE PRODUCTS VERSION



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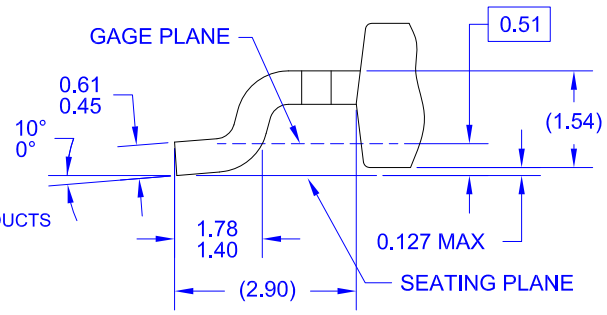
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



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