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March 2012

FSA2267 / FSA2267A
0.35Ω Low-Voltage Dual-SPDT Analog Switch

Features

- Typical 0.35Ω On Resistance (R_{ON}) for +2.7V Supply
- FSA2267A Features <10µA I_{CCT} Current when S Input is Lower than V_{CC}
- R_{ON} Fatness for +2.7V Supply: 0.25Ω Maximum
- 1.6mm x 2.1mm 10-Lead MicroPak™ Package
- Broad V_{CC} Operating Range
- Low THD (0.02% Typical for 32Ω Load)
- High Current Handling Capability (350mA Continuous Current <3.3V Supply)

Applications

- Cell phone
- PDA
- Portable Media Player

Description

The FSA2267 and FSA2267A are Dual Single Pole Double Throw (SPDT) analog switches. The FSA2267 operates from a single 1.65V to 3.6V supply, while the FSA2267A operates from a single 2.3V to 4.3V supply. Each features an ultra-low On Resistance of 0.35Ω at a +2.7V supply and 25°C. Both devices are fabricated with sub-micron CMOS technology to achieve fast switching speeds and designed for break-before-make operation.

FSA2267A features very low quiescent current, even when the control voltage is lower than the V_{CC} supply. This feature services the mobile handset applications very well, allowing for the direct interface with baseband processor general-purpose I/Os.

Ordering Information

Order Number	Top Mark	Package Description	Packing Method
FSA2267L10X	FC	10-Lead MicroPak, 1.6 x 2.1mm, JEDEC MO-255	5000 Units on Tape and Reel
FSA2267AL10X	FD	10-Lead MicroPak, 1.6 x 2.1mm, JEDEC MO-255	5000 Units on Tape and Reel
FSA2267AMUX	FSA 2267A	10-Lead Molded Small Outline Package (MSOP), JEDEC MO-187, 3.0mm Wide	4000 Units on Tape and Reel

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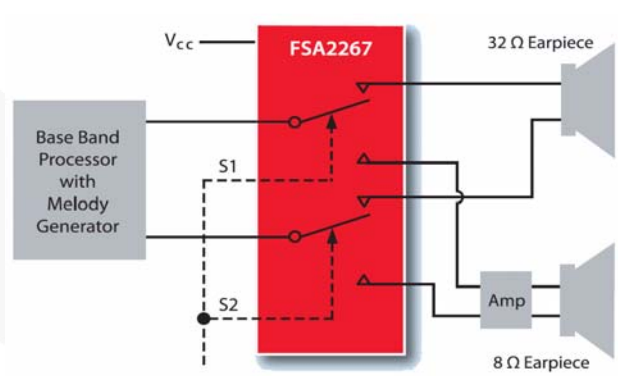


Figure 1. Application Diagram

Analog Symbols

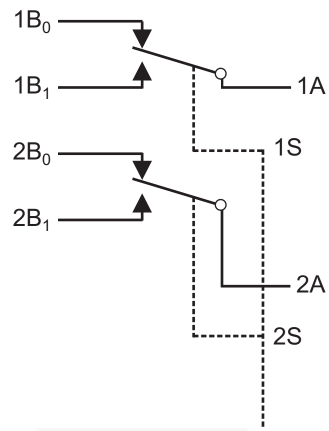


Figure 2. Analog Symbol

Connections Diagram

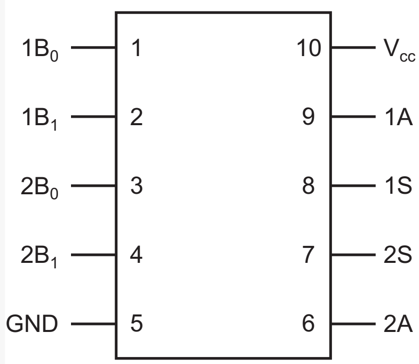


Figure 3. 10-Lead MSOP

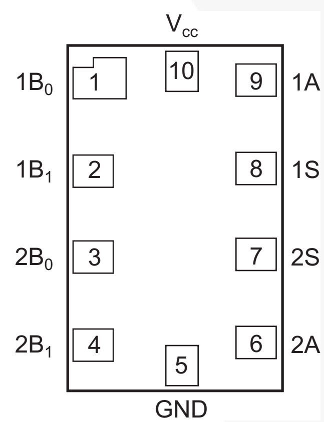


Figure 4. 10-Lead Micropak

Truth Table

Control Input(s)	Function
LOW Logic Level	B_0 Connected to A
HIGH Logic Level	B_1 Connected to A

Pin Descriptions

Pin	Name	Function
1, 2, 3, 4, 6, 9	$1B_0$, $1B_1$, $2B_0$, $2B_1$, 2A, 1A	Data Ports
8, 7	1S, 2S	Control Input
10	VCC	Supply Voltage
5	GND	Ground

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only..

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	-0.5	+5.5	V
V_S	Switch Voltage(1)	-0.5	V_{CC} + 0.5	V
V_{IN}	Control Input Voltage(1)	-0.5	5.5	V
I_{IK}	Input Diode Current(2)	-50		mA
I_{SW}	Switch Current		350	mA
I_{SWPEAK}	Peak Switch Current (Pulsed at 1ms Duration, <10% Duty Cycle)		500	mA
T_{STG}	Storage Temperature Range	-65	+150	°C
T_J	Maximum Junction Temperature		+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)		+260	°C
ESD	Human Body Model: FSA2267		7500	V
	Human Body Model, JESD22-A114:FSA2267A		7000	V
	Charged Device Model, JESD22-C101: FSA2267/FSA2267A		1000	V

Notes:

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.
2. Minimums define the acceptable range of current. Negative current should not exceed minimun negative values.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage			V
	FSA2267	1.65	3.6	V
	FSA2267A	2.3	4.3	
V_{IN}	Control Input Voltage(3)	0	V_{CC}	V
V_{SW}	Switch Input Voltage	0	V_{CC}	V
T_A	Operating Temperature	-40	+85	°C

Note:

3. Unused inputs must be held HIGH or LOW. They may not float.

ESD Protection

ESD Performance of the FSA2267/FSA2267A

FSA2267

- HBM all pins 7.0kV
- CDM all pins 1.0kV

FSA2267A

- HBM all pins 7.5kV
- CDM all pins 1.0kV

Human Body Model

Figure 5 shows the schematic representation of the Human Body Model ESD event. Figure 6 is the ideal waveform representation of the Human Body Model. The device is tested to JEDEC: JESD22-A114 Human Body Model.

Charged Device Model

In manufacturing test and handling environments, a more useful model is the Charged Device Model and the FSA2267/FSA2267A has a very good ESD immunity to this model. The device is tested to JEDEC: JESD22-C101 Charged Device Model.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment and evaluates the equipment in its entirety for ESD immunity. Fairchild Semiconductor has evaluated this device using the IEC 6100-4-2 representative system model depicted in Figure 7.

ESD values measured via the IEC 61000-4-2 evaluation method are influenced by the specific board layout, board size, and many other factors of the manufacturer's product application. Measured system ESD values cannot be guaranteed by Fairchild Semiconductor to exactly correlate to a manufacturer's in-house testing due to these application environment variables. Fairchild Semiconductor has been able to determine that, for ultra-portable applications, an enhanced ESD immunity, relative to the IEC 61000-4-2 specification, can be achieved with the inclusion of a 100Ω–series resistor in the V_{CC} supply path to the analog switch (see Figure 8). Typical improvements of between 3-6kV of ESD immunity (I/O to GND) have been measured with the inclusion of the resistor with the IEC 61000-4-2 representative model. For more information on ESD testing methodologies, please refer to:
AN-6019 Fairchild Analog Switch Products ESD Test Methodology Overview
http://www.fairchildsemi.com/an/AN/AN-6019.pdf.

Additional ESD Test Conditions

For information regarding test methodologies and performance levels, please contact Fairchild Semiconductor.

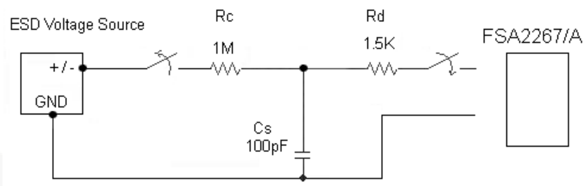


Figure 5. Human Body ESD Test Model

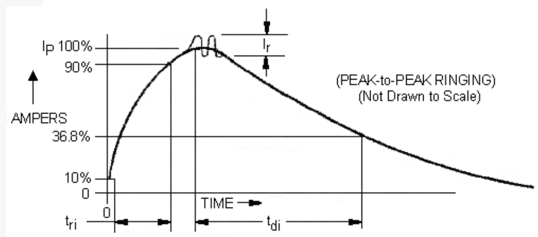


Figure 6. HBM Current Waveform

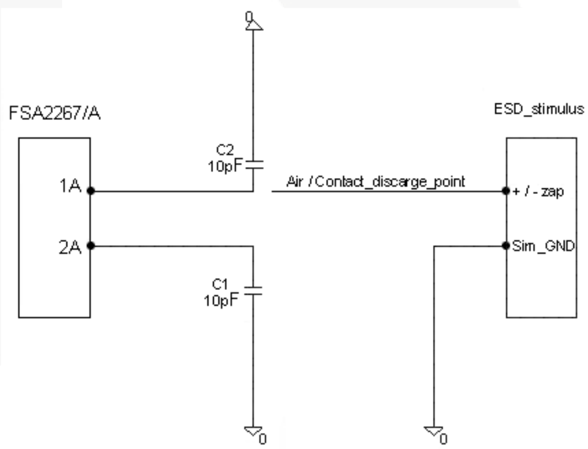


Figure 7. IEC 61000-4-2 ESD Test Model

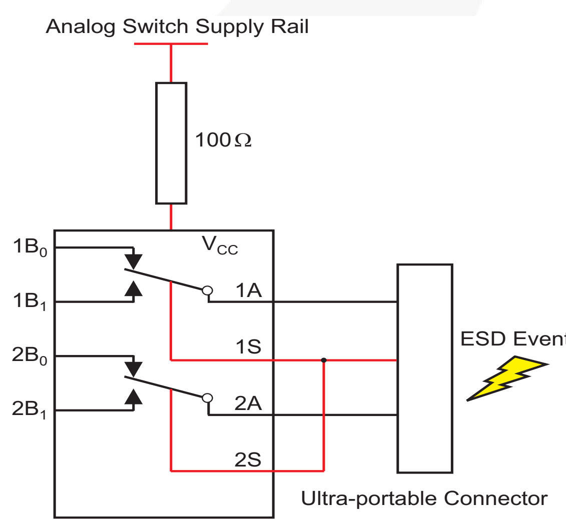


Figure 8. ESD Immunity with 100Ω Resistor

FSA2267 DC Electrical Characteristics

All typical values are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC}	T_A = +25°C			T_A= –40 to +85°C		Units
			(V)	Min.	Typ.	Max.	Min.	Max.	
V_{IH}	Input Voltage High		2.7 to 3.6				2.0		V
			2.3 to 2.7				1.7		
			1.65 to 1.95				0.65 V_{CC}		
V_{IL}	Input Voltage Low		2.7 to 3.6					0.8	V
			2.3 to 2.7					0.7	
			1.65 to 1.95					0.35 V_{CC}	
I_{IN}	Control Input Leakage	V_{IN} = 0V to V_{CC}	1.65 to 3.6				-0.5	0.5	µA
$I_{NO(OFF)}$, $I_{NC(OFF)}$	Off-Leakage Current of Port nB_0 and nB_1	nA = 0.3V, 3.3V, nB_0 or nB_1 = 0.3V, 3.3V or floating	3.6	-5.0		5.0	-50	50	nA
		nA = 0.3V, 2.4V, nB_0 or nB_1 = 0.3V, 2.4V or floating	2.7	-5.0		5.0	-50	50	
		nA = 0.3V, 1.65V, nB_0 or nB_1 = 0.3V, 1.65V or floating	1.95	-5.0		5.0	-50	50	
$I_{A(ON)}$	On Leakage Current of Port 1A and 2A	nA = 0.3V, 3.3V, nB_0 or nB_1 = 0.3V, 3.3V or floating	3.6	-5.0		5.0	-50	50	nA
		nA = 0.3V, 2.4V, nB_0 or nB_1 = 0.3V, 2.4V or floating	2.7	-5.0		5.0	-50	50	
		nA = 0.3V, 1.65V, nB_0 or nB_1 = 0.3V, 1.65V or floating	1.95	-5.0		5.0	-50	50	
R_{ON}	Switch On Resistance(4) See Figure 9	I_{OUT} = 100mA, nB_0 or nB_1 = 0V, 0.7V, 2.0V, 2.7V	2.7		0.35			0.60	Ω
		I_{OUT} = 100mA, nB_0 or nB_1 = 0V, 0.7V, 1.6V, 2.3V	2.3		0.45			0.75	
		I_{OUT} = 100mA, nB_0 or nB_1 = 0.8V	1.65		1.0			3.9	
ΔR_{ON}	On Resistance Matching Between Channels(5)	I_{OUT} = 100mA, nB_0 or nB_1 = 0.7V	2.7		0.040			0.075	Ω
			2.3		0.040			0.080	
			1.65		0.1				
$R_{FLAT(ON)}$	On Resistance Flatness(6)	I_{OUT} = 100mA, nB_0 or nB_1 = 0V to V_{CC}	2.7					0.25	Ω
			2.3					0.3	
			1.65		0.3				
I_{CC}	Quiescent Supply Current	V_{IN} = 0V or V_{CC}, I_{OUT} = 0A	3.6	-100		100	-500	500	nA

Notes:

4. On resistance is determined by the voltage drop between A and B pins at the indicated current through the switch.
5. $\Delta R_{ON} = R_{ONmax} - R_{ONmin}$ measured at identical V_{CC}, temperature, and voltage.
6. Flatness is defined as the difference between the maximum and minimum value of R_{ON} over the specified range of conditions.

FSA2267A DC Electrical Characteristics

All typical values are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC}	T_A = +25°C			T_A= –40 to +85°C		Units
			(V)	Min.	Typ.	Max.	Min.	Max.	
V_{IH}	Input Voltage High		3.6 to 4.3				1.7		V
			2.7 to 3.6				1.5		
			2.3 to 2.7				1.4		
V_{IL}	Input Voltage Low		3.6 to 4.3					0.7	V
			2.7 to 3.6					0.5	
			2.3 to 2.7					0.4	
I_{IN}	Control Input Leakage	V_{IN} = 0V to V_{CC}	2.3 to 4.3				-0.5	0.5	µA
$I_{NO(OFF)}$, $I_{NC(OFF)}$	Off-Leakage Current of Port nB_0 and nB_1	nA = 0.3V, 4.0V, nB_0 or nB_1 = 4.0V, 0.3V or floating	4.3	-10.0		10.0	-100	100	nA
		nA = 0.3V, 3.3V, nB_0 or nB_1 = 0.3V, 3.3V or floating	3.6	-5.0		5.0	-50	50	
		nA = 0.3V, 2.4V, nB_0 or nB_1 = 0.3V, 2.4V or floating	2.7	-5.0		5.0	-50	50	
$I_{A(ON)}$	On Leakage Current of Port 1A and 2A	nA = 0.3V, 4.0V, nB_0 or nB_1 = 0.3V, 4.0V or floating	4.3	-20.0		20.0	-200	200	nA
		nA = 0.3V, 3.3V, nB_0 or nB_1 = 0.3V, 3.3V or floating	3.6	-5.0		5.0	-50	50	
		nA = 0.3V, 3.3V, nB_0 or nB_1 = 0.3V, 3.3V or floating	2.7	-5.0		5.0	-50	50	
R_{ON}	Switch On Resistance[7]	I_{OUT} = 100mA, nB_0 or nB_1 = 0V, 0.7V, 3.6V, 4.3V	4.3		0.35			0.6	Ω
		I_{OUT} = 100mA, nB_0 or nB_1 = 0V, 0.7V, 2.3V, 3.0V	3.0		0.35			0.6	
		I_{OUT} = 100mA, nB_0 or nB_1 = 0V, 0.7V, 2.0V, 2.7V	2.7		0.35			0.6	
		I_{OUT} = 100mA, nB_0 or nB_1 = 0.8V	1.65		1.0				
ΔR_{ON}	On Resistance Matching Between Channels[8] See Figure 10	I_{OUT} = 100mA, nB_0 or nB_1 = 0.7V	4.3		0.04			0.075	Ω
			3.0		0.04			0.075	
			2.7		0.04			0.075	
			1.65		0.1				
$R_{FLAT(ON)}$	On Resistance Flatness[9]	I_{OUT} = 100mA, nB_0 or nB_1 = 0V to V_{CC}	4.3		0.15			0.25	Ω
			3.0		0.15			0.25	
			2.7		0.15			0.25	
			1.65		0.3				
I_{CC}	Quiescent Supply Current	V_{IN} = 0V or V_{CC}, I_{OUT} = 0A	4.3	-100	80	100	-500	500	nA
I_{CCT}	Increase in I_{CC} per Input	V_{IN} = 1.8V	4.3		7.0	10.0		15.0	µA
		V_{IN} = 2.6V			0.5	2.0		7.0	

Notes:

7. On resistance is determined by the voltage drop between A and B pins at the indicated current through the switch.
8. $\Delta R_{ON} = R_{ONmax} - R_{ONmin}$ measured at identical V_{CC}, temperature, and voltage.
9. Flatness is defined as the difference between the maximum and minimum value of R_{ON} over the specified range of conditions.

FSA2267 AC Electrical Characteristics

All typical values are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = +25°C			T_A= -40 to +85°C		Units	Figure Number
				Min.	Typ.	Max.	Min.	Max.		
t_{ON}	Turn-On Time	nB_0 or nB_1 = 1.5V, R_L = 50Ω, C_L = 35 pF	2.7 to 3.6		30.0	38.0		42.0	ns	Figure 11
			2.3 to 2.7		29.0	37.0		40.0		
			1.65 to 1.95		27.0	35.0		38.0		
t_{OFF}	Turn-Off Time	nB_0 or nB_1 = 1.5V, R_L = 50Ω, C_L = 35 pF	2.7 to 3.6		13.0	16.0		18.0	ns	Figure 11
			2.3 to 2.7		14.0	18.0		20.0		
			1.65 to 1.95		15.0	21.0		25.0		
t_{BBM}	Break-Before-Make Time	nB_0 or nB_1 = 1.5V, R_L = 50Ω, C_L = 35 pF	2.7 to 3.6		17.0		2.0		ns	Figure 12
			2.3 to 2.7		15.0		2.0			
			1.65 to 1.95		12.0		2.0			
Q	Charge Injection	C_L = 100 pF, V_{GEN} = 0V, R_{GEN} = 0Ω	2.7 to 3.6		9.0				pC	Figure 14
		C_L = 100 pF, V_{GEN} = 0V, R_{GEN} = 0Ω	2.3 to 2.7		9.0					
		C_L = 100 pF, V_{GEN} = 0V, R_{GEN} = 0Ω	1.65 to 1.95		9.0					
OIRR	Off Isolation	f = 100kHz, R_L = 50Ω, C_L = 5pF (Stray)	2.7 to 3.6		-80.0				dB	Figure 13
			2.3 to 2.7		-80.0					
			1.65 to 1.95		-80.0					
Xtalk	Crosstalk	f = 100kHz, R_L = 50Ω, C_L = 5pF (Stray)	2.7 to 3.6		-80.0				dB	Figure 13
			2.3 to 2.7		-80.0					
			1.65 to 1.95		-80.0					
BW	-3db Bandwidth	R_L = 50Ω	1.65 to 3.6		45.0				MHz	Figure 16
THD	Total Harmonic Distortion	R_L = 32Ω, V_{IN} = $2V_{pk-pk}$, f = 20Hz to 20kHz	2.7 to 3.6		0.024				%	Figure 17
		R_L = 32Ω, V_{IN} = $1.5V_{pk-pk}$, f = 20Hz to 20kHz	2.3 to 2.7		0.015					
		R_L = 32Ω, V_{IN} = $1.2V_{pk-pk}$, f = 20Hz to 20kHz	1.65 to 1.95		0.35					

FSA2267A AC Electrical Characteristics

All typical value are at 25°C unless otherwise specified.

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = +25°C			T_A= -40 to +85°C		Units	Figure Number
				Min.	Typ.	Max.	Min.	Max.		
t_{ON}	Turn-On Time	nB_0 or nB_1 = 1.5V, R_L = 50Ω, C_L = 35pF	3.6 to 4.3		37.0	46.0		48.0	ns	Figure 11
			2.7 to 3.6		37.0	50.0		57.0		
			2.3 to 2.7		60					
			1.65		570					
t_{OFF}	Turn-Off Time	nB_0 or nB_1 = 1.5V, R_L = 50Ω, C_L = 35pF	3.6 to 4.3		15.0	23.0		25.0	ns	Figure 11
			2.7 to 3.6		16.0	30.0		30.0		
			2.3 to 2.7		50.0					
			1.65		500					
t_{BBM}	Break-Before-Make Time	nB_0 or nB_1 = 1.5V, R_L = 50Ω, C_L = 35pF	3.6 to 4.3		8.0		2.0		ns	Figure 12
			2.7 to 3.6		8.0		2.0			
			2.3 to 2.7		8.0		2.0			
Q	Charge Injection	C_L = 100 pF, V_{GEN} = 0V, R_{GEN} = 0Ω	3.6 to 4.3		24.0				pC	Figure 14
		C_L = 100 pF, V_{GEN} = 0V, R_{GEN} = 0Ω	2.7 to 3.6		24.0					
		C_L = 100 pF, V_{GEN} = 0V, R_{GEN} = 0Ω	2.3 to 2.7		24.0					
OIRR	Off Isolation	f = 100kHz, R_L = 50Ω, C_L = 5pF (Stray)	3.6 to 4.3		-75.0				dB	Figure 13
			2.7 to 3.6		-75.0					
			2.3 to 2.7		-75.0					
Xtalk	Crosstalk	f = 100kHz, R_L = 50Ω, C_L = 5pF (Stray)	3.6 to 4.3		-70.0				dB	Figure 13
			2.7 to 3.6		-70.0					
			2.3 to 2.7		-70.0					
BW	-3db Bandwidth	R_L = 50Ω	2.3 to 4.3		45.0				MHz	Figure 16
THD	Total Harmonic Distortion	R_L = 32Ω, V_{IN} = 2V_{pk-pk}, f = 20Hz to 20kHz	3.6 to 4.3		0.02				%	Figure 17
		R_L = 32Ω, V_{IN} = 1.5V_{pk-pk}, f = 20Hz to 20kHz	2.7 to 3.6		0.02					
		R_L = 32Ω, V_{IN} = 1.2V_{pk-pk}, f = 20Hz to 20kHz	2.3 to 2.7		0.02					

Capacitance

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = +25°C			T_A= -40 to +85°C		Units	Figure Number
				Min.	Typ.	Max.	Min.	Max.		
C_{IN}	Control Pin Input Capacitance	f = 1Mhz	0.0		1.5				pF	Figure 15
C_{OFF}	B Port Off Capacitance	f = 1Mhz	3.3		30.0				pF	Figure 15
C_{ON}	A Port On Capacitance	f = 1Mhz	3.3		126				pF	Figure 15

Typical Characteristics

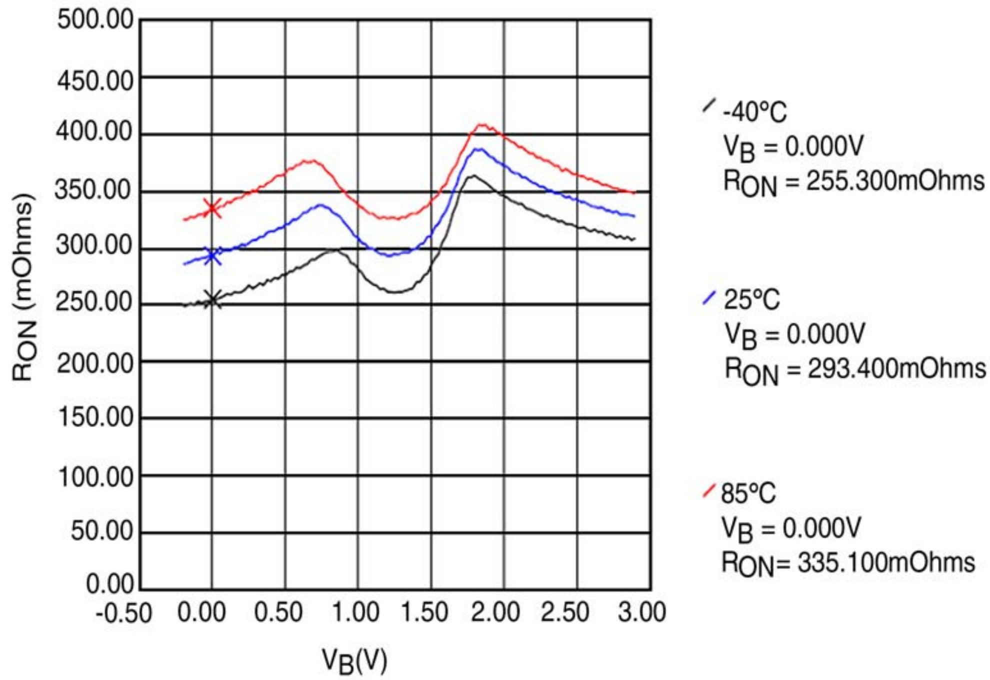


Figure 9. R_{ON} at 2.7V for FSA2267

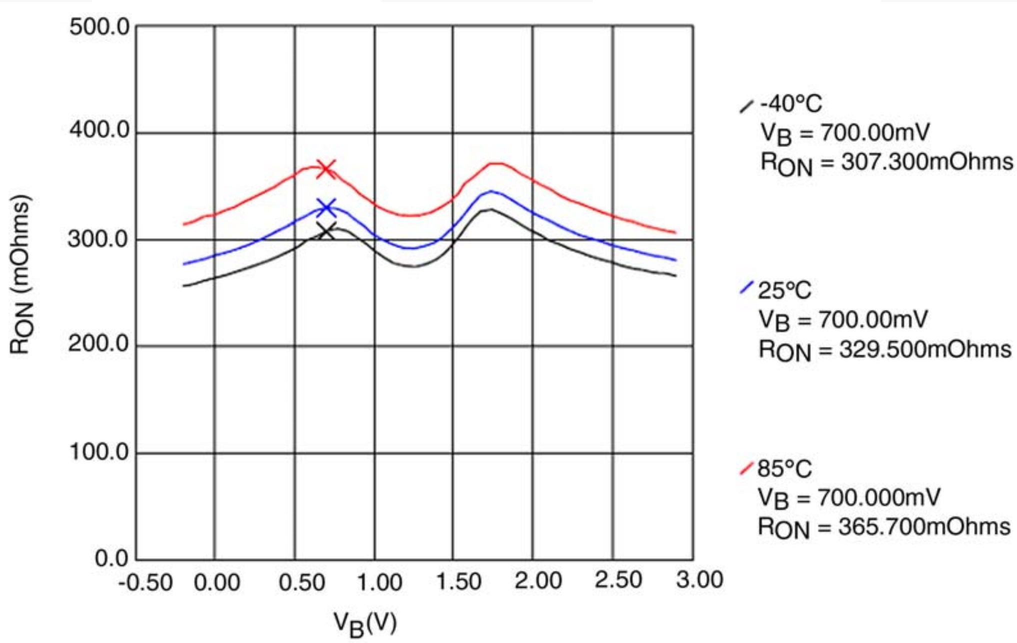
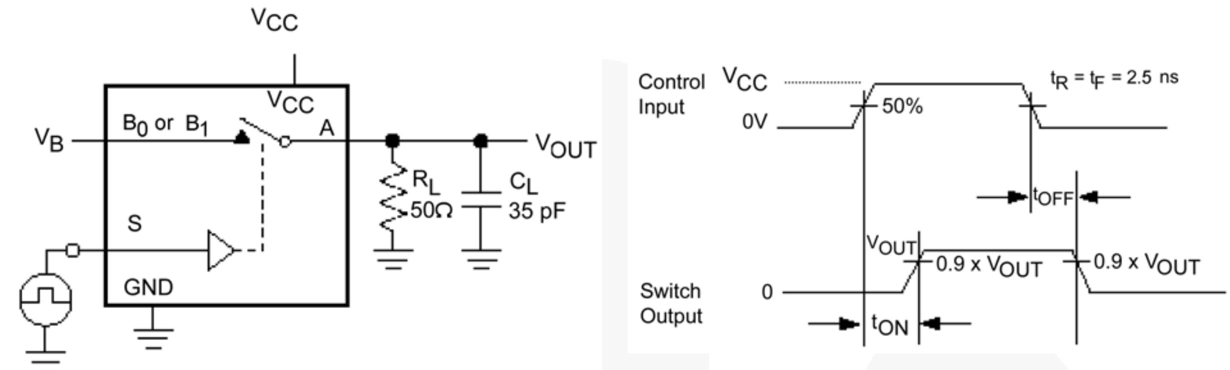


Figure 10. R_{ON} at 2.7V for FSA2267A

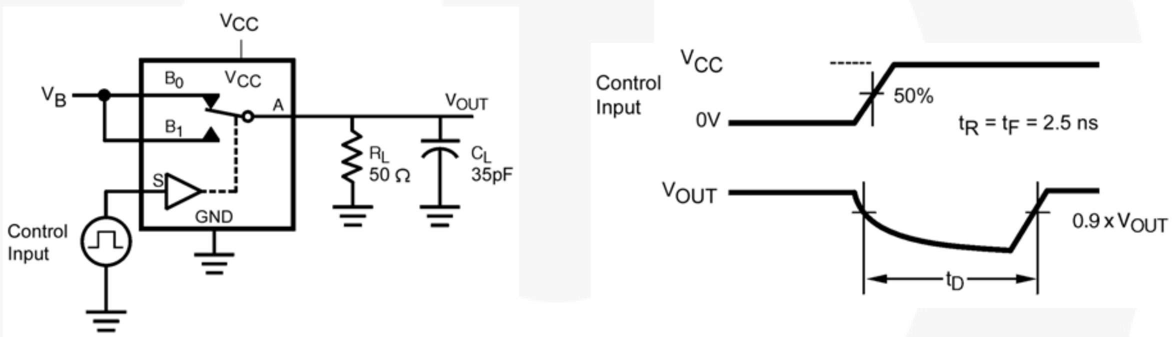
AC Loading and Waveforms



C_L includes Fixture and Stray Capacitance.

Logic input waveforms are inverted for switches with opposite logic sense.

Figure 11. Turn-On/Turn-Off Timing



C_L Includes Fixture and Stray Capacitance

Figure 12. Break-Before-Make Timing

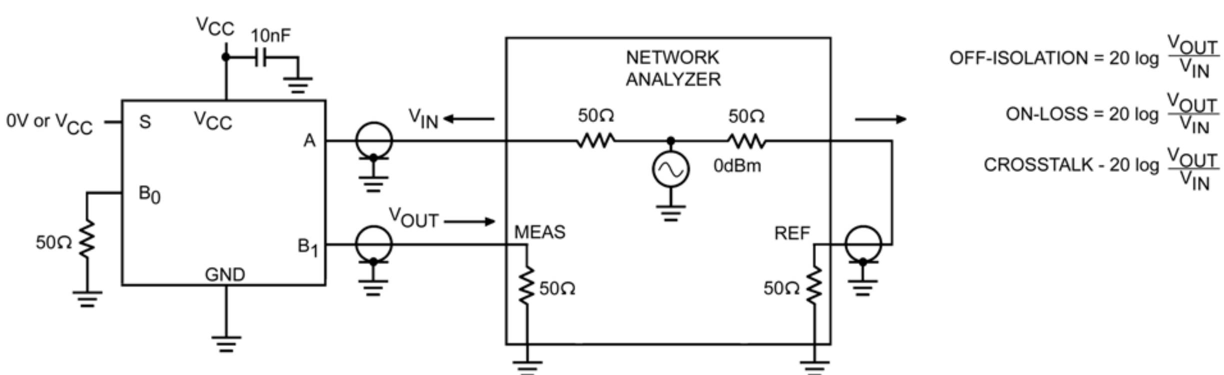
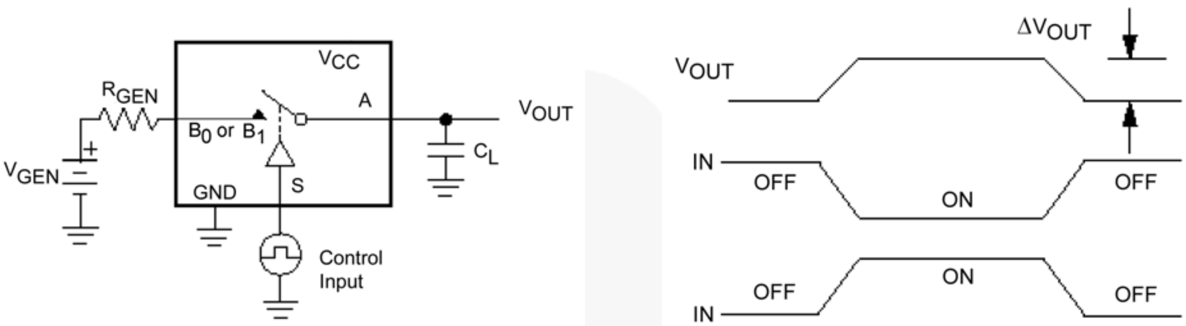


Figure 13. Off Isolation and Crosstalk

AC Loading and Waveforms (Continued)



$Q = (DV_{OUT})(C_L)$

Figure 14. Charge Injection

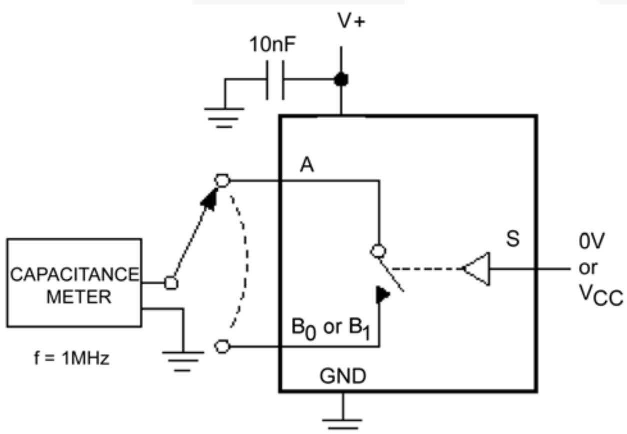


Figure 15. On/Off Capacitance Measurement Setup

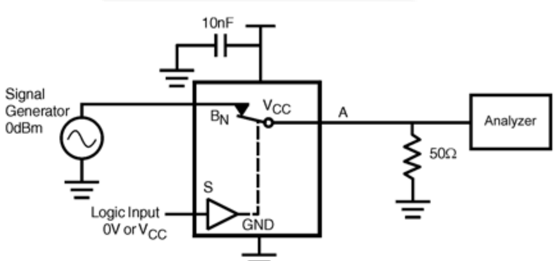


Figure 16. Bandwidth

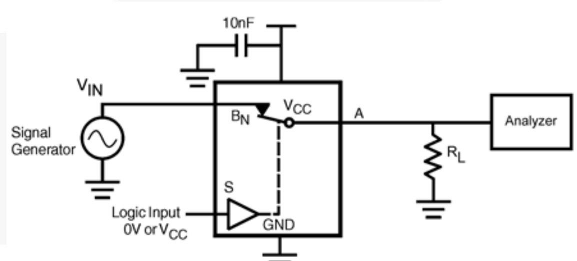
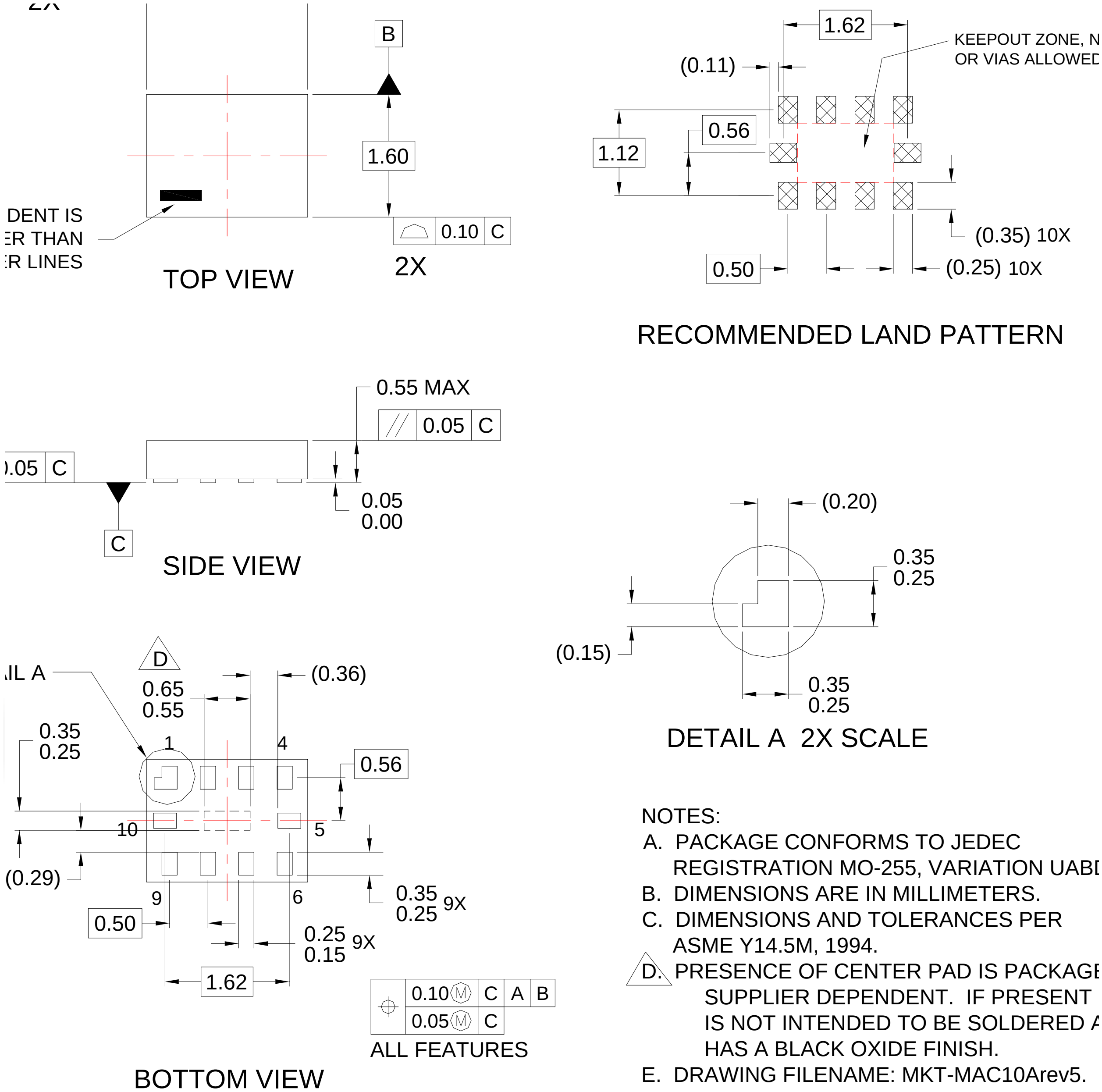


Figure 17. Harmonic Distortion

Physical Dimensions



NOTES:

A. PACKAGE CONFORMS TO JEDEC REGISTRATION MO-255, VARIATION UABI

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

D. PRESENCE OF CENTER PAD IS PACKAGE SUPPLIER DEPENDENT. IF PRESENT IS NOT INTENDED TO BE SOLDERED A HAS A BLACK OXIDE FINISH.

E. DRAWING FILENAME: MKT-MAC10Arev5.

Figure 18. 10-Lead, MicroPak™, 1.6 x 2.1mm

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Physical Dimensions

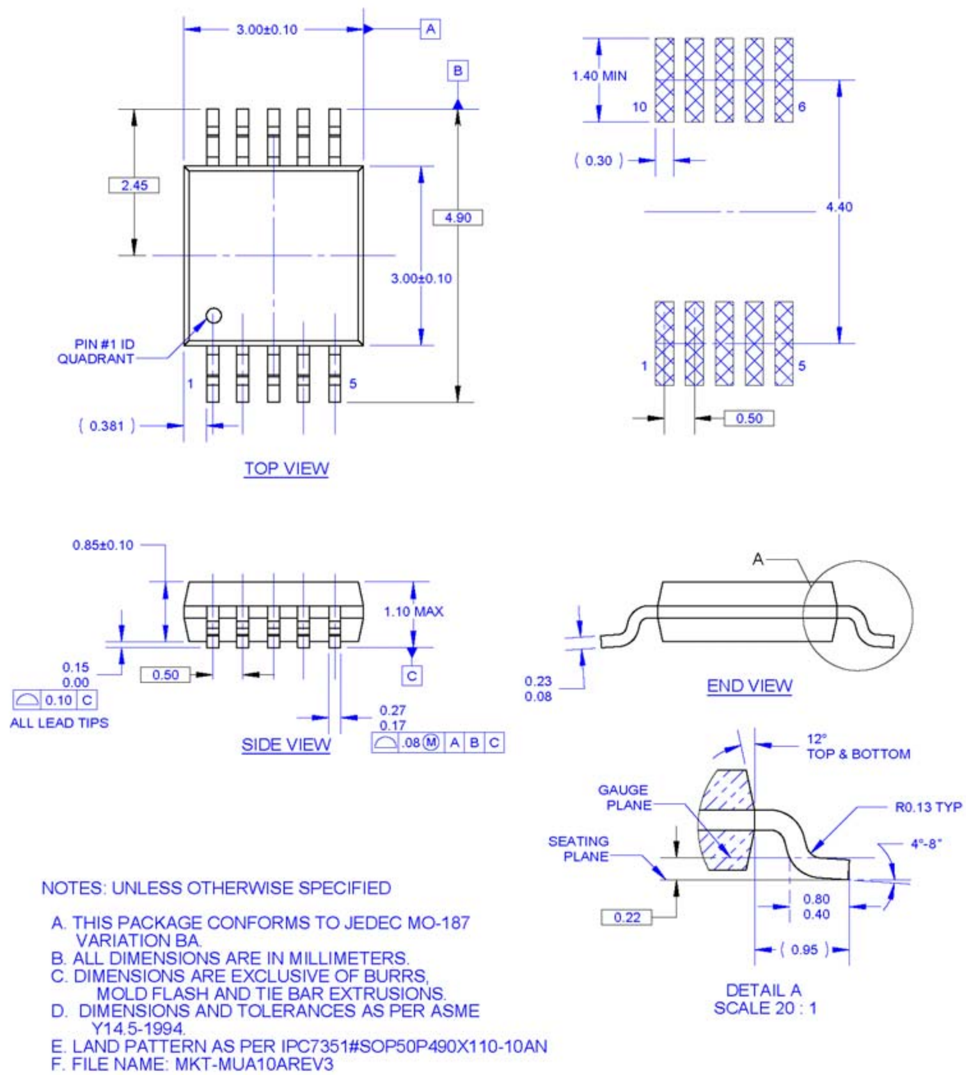

Figure 19. Pb-Free, 10-Lead, Molded Small Outline Package (MSOP), JEDEC MO-187, 3.0mm Wide

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