

High and Low Side Driver

Features

- Floating channel designed for bootstrap operation
- Fully operational to +1200 V
- Tolerant to negative transient voltage
- dV/dt immune
- Gate drive supply range from 12 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V logic compatible
- Separate logic supply range from 3.3 V to 20 V
- Logic and power ground ± 5 V offset
- CMOS Schmitt-triggered inputs with pull-down
- Cycle by cycle edge-triggered shutdown logic
- Matched propagation delay for both channels
- Outputs in phase with inputs

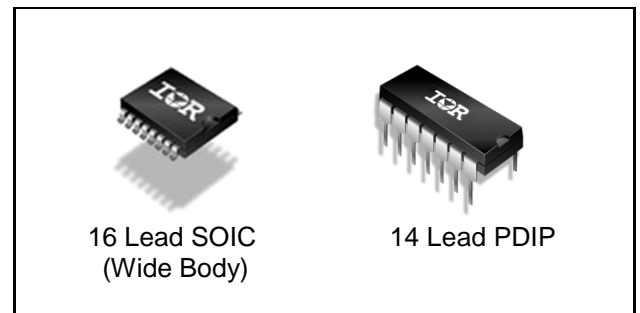
Description

The IR2213(S) is a high voltage, high speed power MOSFET and IGBT driver with independent high and low side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. Logic inputs are compatible with standard CMOS or LSTTL outputs, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 1200 V.

Product Summary

| | |
|-------------------------------|-----------------|
| V_{OFFSET} (max) | 1200 V |
| $I_{\text{O+/-}}$ | 1.7 A / 2 A |
| V_{OUT} | 12 V – 20 V |
| $t_{\text{on/off}}$ (typical) | 280 ns / 225 ns |
| Delay Matching | 30 ns |

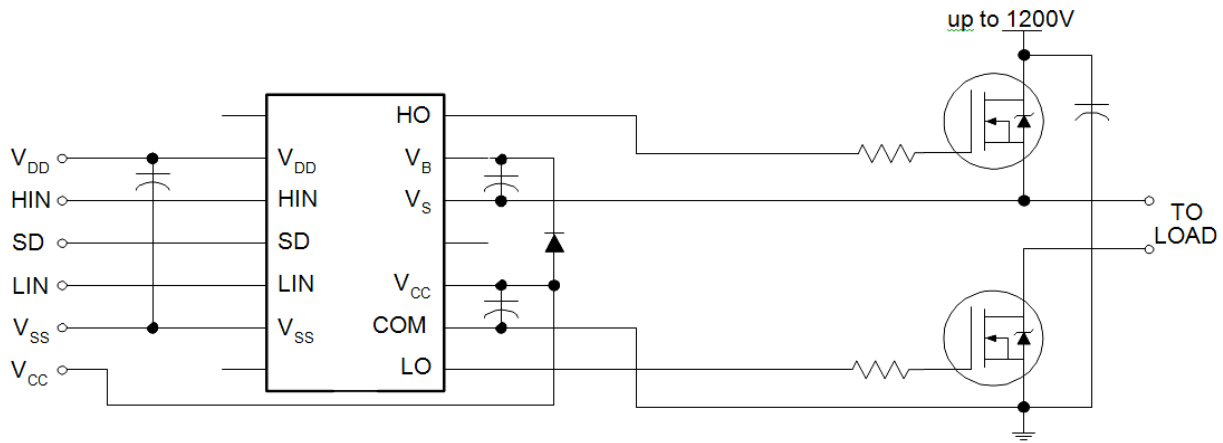
Package Options



Ordering Information

| Base Part Number | Package Type | Standard Pack | | Orderable Part Number |
|------------------|--------------|---------------|----------|-----------------------|
| | | Form | Quantity | |
| IR2213SPBF | SO16WB | Tube | 45 | IR2213SPBF |
| IR2213SPBF | SO16WB | Tape and Reel | 1000 | IR2213STRPBF |
| IR2213PBF | PDIP14 | Tube | 25 | IR2213PBF |

Typical Connection Diagram



Refer to Lead Assignments for correct pin configuration. This/These diagram(s) show electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The Thermal Resistance and Power Dissipation ratings are measured under board mounted and still air conditions.

| Symbol | Definition | Min. | Max. | Units | |
|------------|---|----------------|----------------|------------------|--------------------|
| V_B | High Side Floating Supply Voltage | -0.3 | 1225 | V | |
| V_S | High Side Floating Supply Offset Voltage | $V_B - 25$ | $V_B + 0.3$ | | |
| V_{HO} | High Side Floating Output Voltage | $V_S - 0.3$ | $V_B + 0.3$ | | |
| V_{CC} | Low Side Fixed Supply Voltage | -0.3 | 25 | | |
| V_{LO} | Low Side Output Voltage | -0.3 | $V_{CC} + 0.3$ | | |
| V_{DD} | Logic Supply Voltage | -0.3 | $V_{SS} + 25$ | | |
| V_{SS} | Logic Supply Offset Voltage | $V_{CC} - 25$ | $V_{CC} + 0.3$ | | |
| V_{IN} | Logic Input Voltage (HIN, LIN & SD) | $V_{SS} - 0.3$ | $V_{DD} + 0.3$ | | |
| dVs/dt | Allowable Offset Supply Voltage Transient (Figure 2) | — | 50 | V/ns | |
| P_D | Package Power Dissipation @ $T_A \leq +25^\circ\text{C}$ | (14 Lead PDIP) | — | 1.3 | W |
| | | (16 Lead SOIC) | — | 1.0 | |
| R_{THJA} | Thermal Resistance, Junction to Ambient | (14 Lead PDIP) | — | 75 | $^\circ\text{C/W}$ |
| | | (16 Lead SOIC) | — | 100 | |
| T_J | Junction Temperature | — | 125 | $^\circ\text{C}$ | |
| T_S | Storage Temperature | -55 | 150 | | |
| T_L | Lead Temperature (Soldering, 10 seconds) | — | 300 | | |

Recommended Operating Conditions

The Input / Output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset ratings are tested with all supplies biased at 15 V differential.

| Symbol | Definition | Min. | Max. | Units |
|----------|--|------------------|---------------|-------|
| V_B | High Side Floating Supply Absolute Voltage | $V_S + 12$ | $V_S + 20$ | V |
| V_S | High Side Floating Supply Offset Voltage | † | 1200 | |
| V_{HO} | High Side Floating Output Voltage | V_S | V_B | |
| V_{CC} | Low Side Fixed Supply Voltage | 12 | 20 | |
| V_{LO} | Low Side Output Voltage | 0 | V_{CC} | |
| V_{DD} | Logic Supply Voltage | $V_{SS} + 3$ | $V_{SS} + 20$ | |
| V_{SS} | Logic Supply Offset Voltage | -5 ^{††} | 5 | |
| V_{IN} | Logic Input Voltage (HIN, LIN & SD) | V_{SS} | V_{DD} | |

† Logic operational for V_S of -5 to +1200V. Logic state held for V_S of -5V to $-V_{BS}$. (Please refer to the Design Tip DT97-3 for more details).

†† When $V_{DD} < 5V$, the minimum V_{SS} offset is limited to $-V_{DD}$

Dynamic Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15 V, C_L = 1000 pF, T_A = 25 °C and V_{SS} = COM unless otherwise specified. The dynamic electrical characteristics are measured using the test circuit shown in Figure 3.

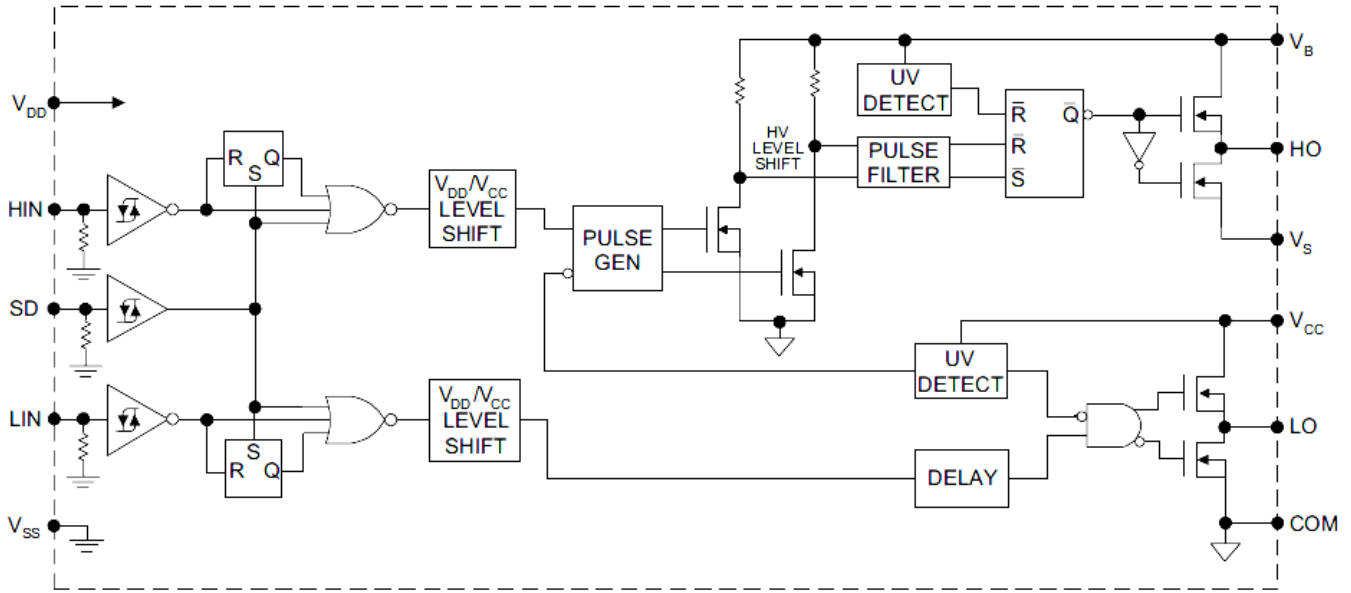
| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|-----------|-------------------------------------|------|------|------|-------|-----------------|
| t_{on} | Turn-On Propagation Delay | — | 280 | — | ns | $V_S = 0V$ |
| t_{off} | Turn-Off Propagation Delay | — | 225 | — | | $V_S = 1200V$ |
| t_{sd} | Shutdown Propagation Delay | — | 230 | — | | $V_S = 1200V$ |
| t_r | Turn-On Rise Time | — | 25 | — | | |
| t_f | Turn-Off Fall Time | — | 17 | — | | |
| MT | Delay Matching, HS & LS Turn-On/Off | — | — | 30 | | |

Static Electrical Characteristics

V_{BIAS} (V_{CC} , V_{BS} , V_{DD}) = 15 V, T_A = 25 °C and V_{SS} = COM unless otherwise specified. The V_{IN} , V_{TH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The V_O and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

| Symbol | Definition | Min. | Typ. | Max. | Units | Test Conditions |
|-------------|---|------|------|------|---------------|---|
| V_{IH} | Logic "1" Input Voltage | 9.5 | — | — | V | |
| V_{IL} | Logic "0" Input Voltage | — | — | 6.0 | | |
| V_{OH} | High Level Output Voltage, $V_{BIAS} - V_O$ | — | — | 1.2 | | $I_O = 0A$ |
| V_{OL} | Low Level Output Voltage, V_O | — | — | 0.1 | | $I_O = 0A$ |
| I_{LK} | Offset Supply Leakage Current | — | — | 50 | μA | $V_B = V_S = 1200V$ |
| I_{QBS} | Quiescent V_{BS} Supply Current | — | 125 | 230 | | $V_{IN} = 0V$ or V_{DD} |
| I_{QCC} | Quiescent V_{CC} Supply Current | — | 180 | 340 | | $V_{IN} = 0V$ or V_{DD} |
| I_{QDD} | Quiescent V_{DD} Supply Current | — | 15 | 30 | | $V_{IN} = 0V$ or V_{DD} |
| I_{IN+} | Logic "1" Input Bias Current | — | 20 | 40 | | $V_{IN} = V_{DD}$ |
| I_{IN-} | Logic "0" Input Bias Current | — | — | 1.0 | $V_{IN} = 0V$ | |
| V_{BSUV+} | V_{BS} Supply Undervoltage Positive Going Threshold | 8.7 | 10.2 | 11.7 | V | |
| V_{BSUV-} | V_{BS} Supply Undervoltage Negative Going Threshold | 7.9 | 9.3 | 10.7 | | |
| V_{CCUV+} | V_{CC} Supply Undervoltage Positive Going Threshold | 8.7 | 10.2 | 11.7 | | |
| V_{CCUV-} | V_{CC} Supply Undervoltage Negative Going Threshold | 7.9 | 9.3 | 10.7 | | |
| I_{O+} | Output High Short Circuit Pulsed Current | 1.7 | 2.0 | — | A | $V_O = 0V, V_{IN} = V_{DD}$ $PW \leq 10 \mu s$ |
| I_{O-} | Output Low Short Circuit Pulsed Current | 2.0 | 2.5 | — | | $V_O = 15V, V_{IN} = 0V$ $PW \leq 10 \mu s$ |

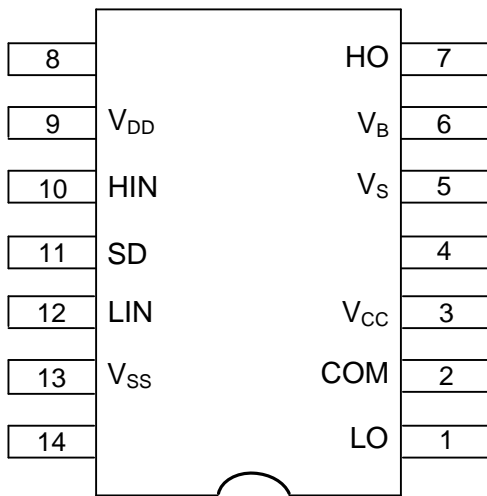
Functional Block Diagram



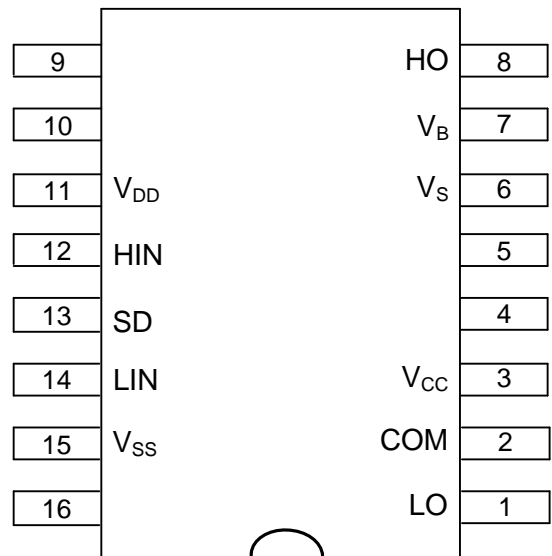
Lead Definitions

| Symbol | Description |
|-----------------|---|
| V _{DD} | Logic Supply |
| HIN | Logic Input for High Side Gate Driver Output (HO), In Phase |
| SD | Logic Input for Shutdown |
| LIN | Logic Input for Low Side Gate Driver Output (LO), In Phase |
| V _{SS} | Logic Ground |
| V _B | High Side Floating Supply |
| HO | High Side Gate Drive Output |
| V _S | High Side Floating Supply Return |
| V _{CC} | Low Side Supply |
| LO | Low Side Gate Drive Output |
| COM | Low Side Return |

Lead Assignments



14-Lead PDIP



16-Lead SOIC
(Wide Body)

Application Information and Additional Information

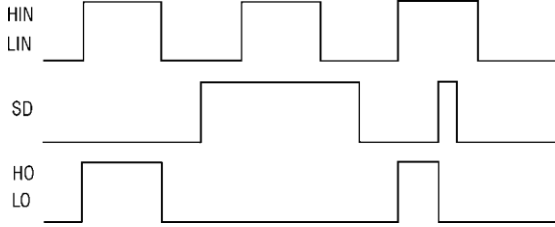


Figure 1. Input / Output Timing Diagram

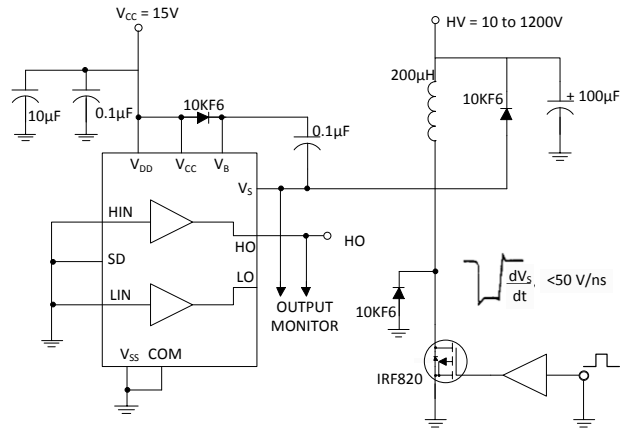


Figure 2. Floating Supply Voltage Transient Test Circuit

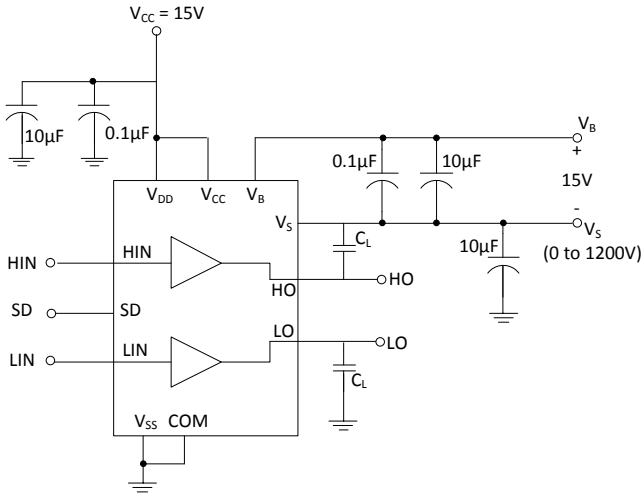


Figure 3. Switching Time Test Circuit

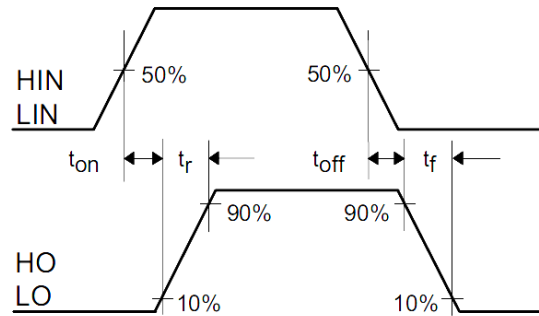


Figure 4. Switching Time Waveform Definition

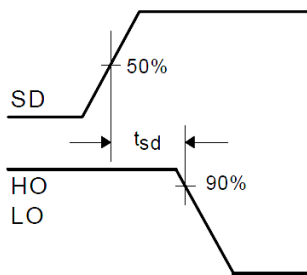


Figure 5. Shutdown Waveform Definitions

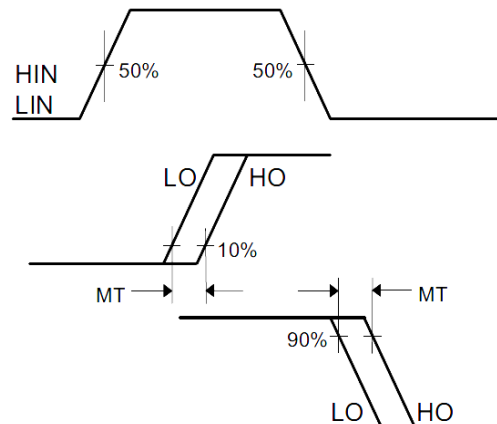


Figure 6. Delay Matching Waveform Definitions

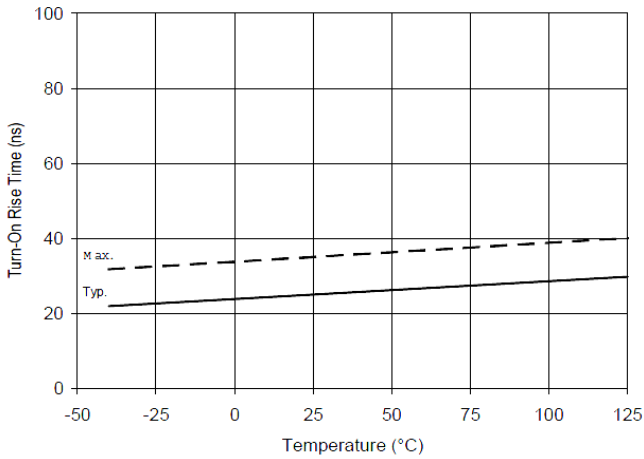


Figure 7A. Turn-On Rise Time vs. Temperature

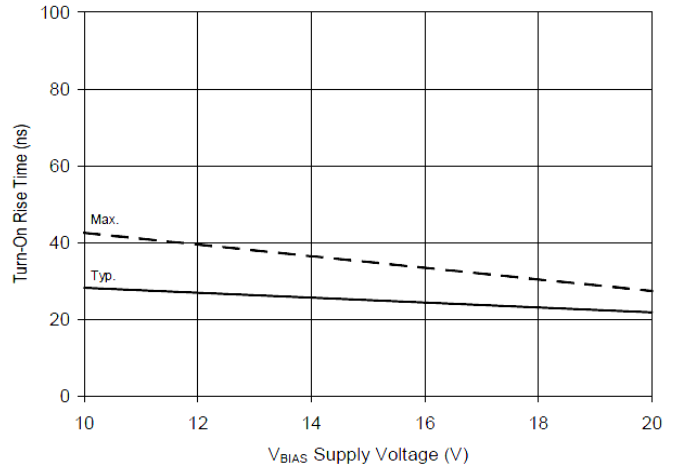


Figure 7B. Turn-On Rise Time vs. Voltage

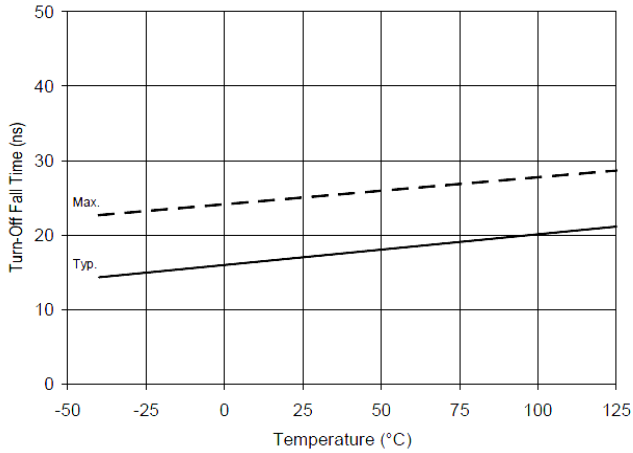


Figure 8A. Turn-Off Fall Time vs. Temperature

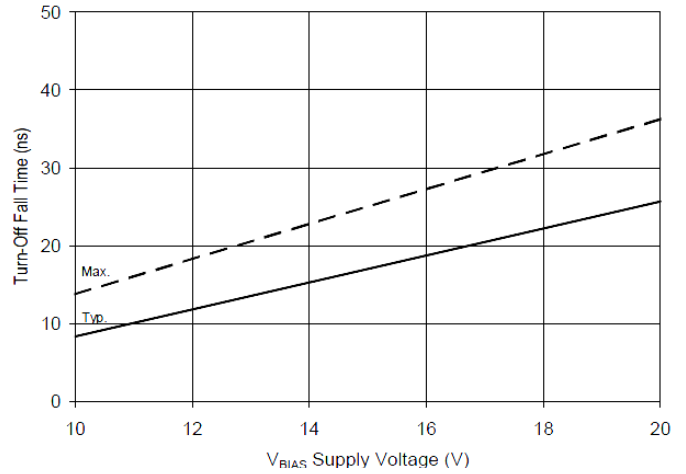


Figure 8B. Turn-Off Fall Time vs. Voltage

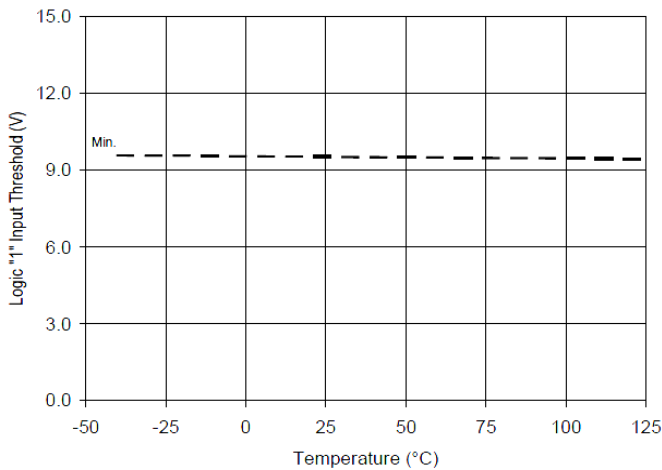


Figure 9A. Logic "1" Input Threshold vs. Temperature

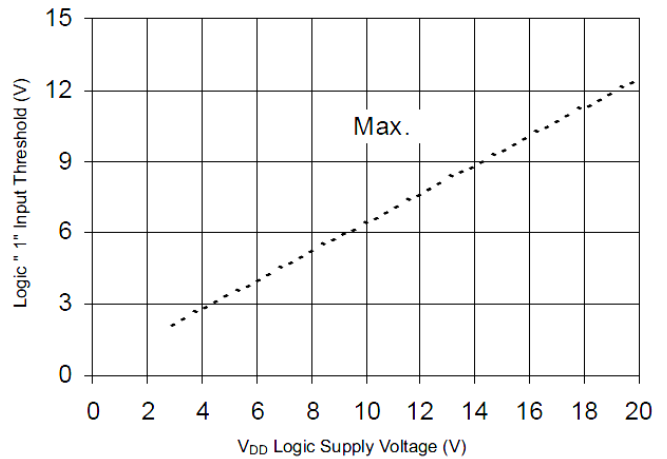


Figure 9B. Logic "1" Input Threshold vs. Voltage

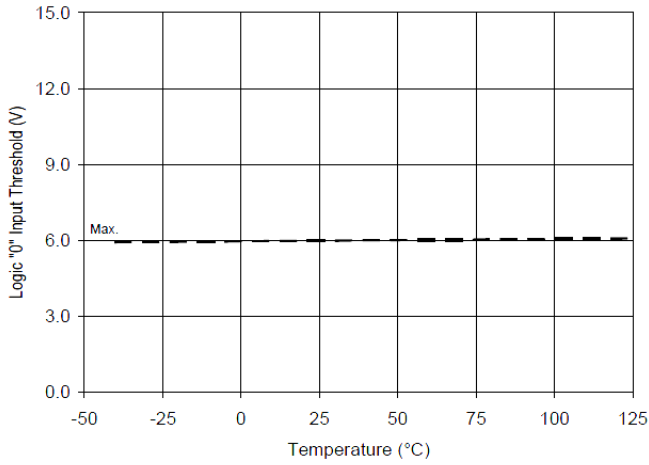


Figure 10A. Logic "0" Input Threshold vs. Temperature

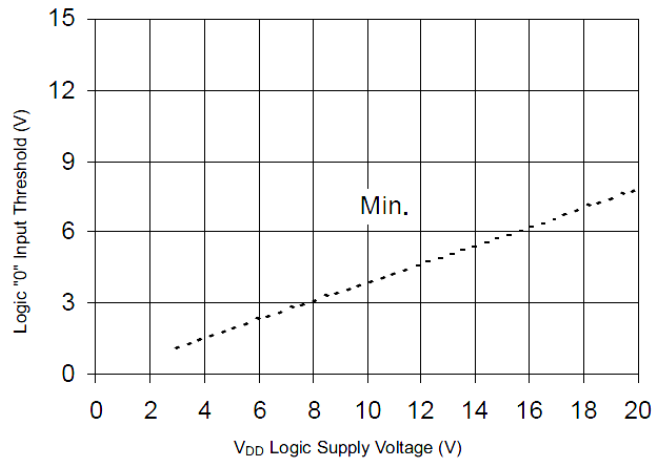


Figure 10B. Logic "0" Input Threshold vs. Voltage

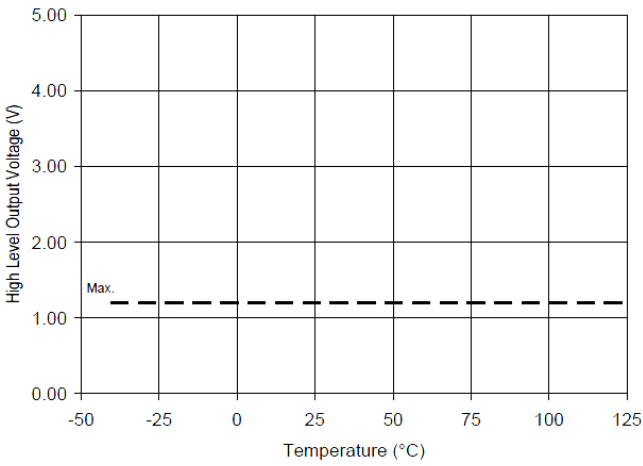


Figure 11A. High Level Output vs. Temperature

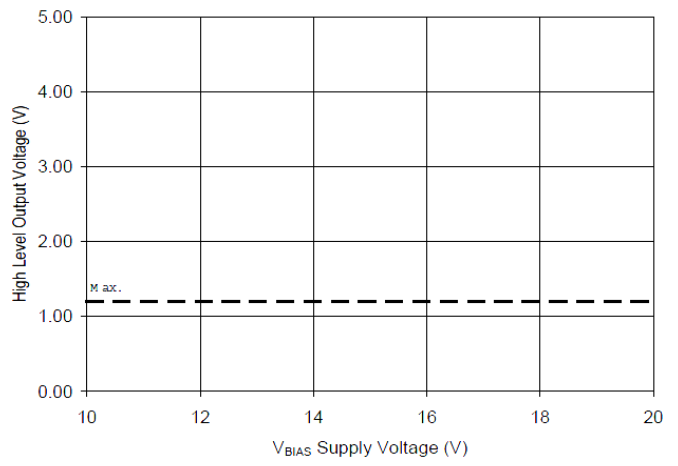


Figure 11B. High Level Outputs vs. Voltage

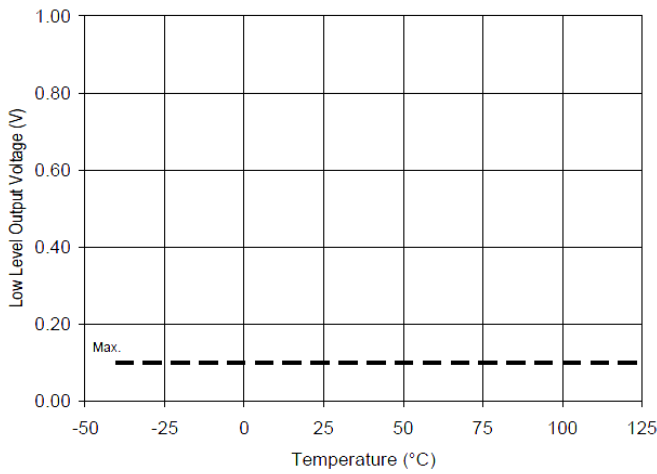


Figure 12A. Low Level Output vs. Temperature

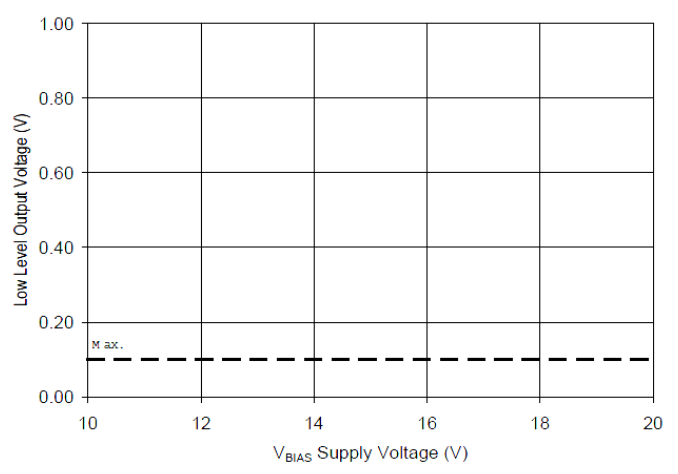


Figure 12B. Low Level Output vs. Voltage

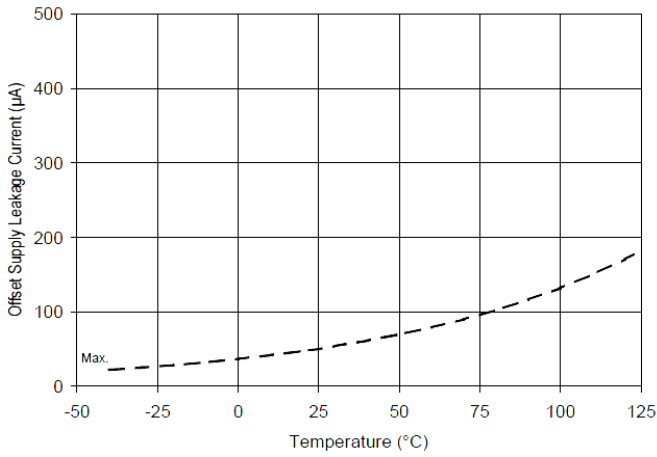


Figure 13A. Offset Supply Current vs. Temperature

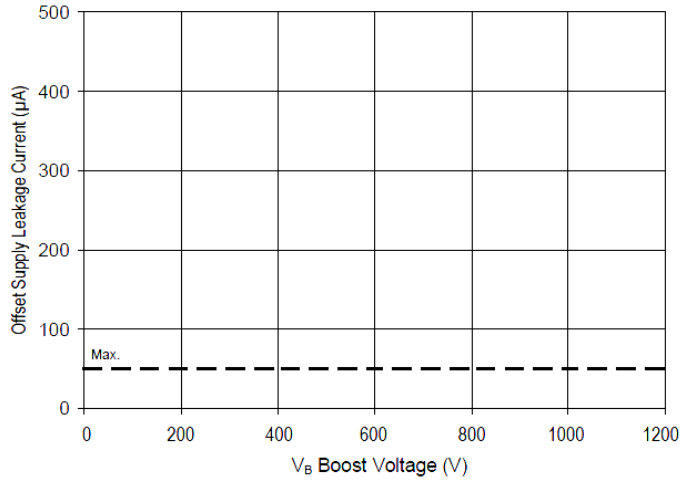


Figure 13B. Offset Supply Current vs. Voltage

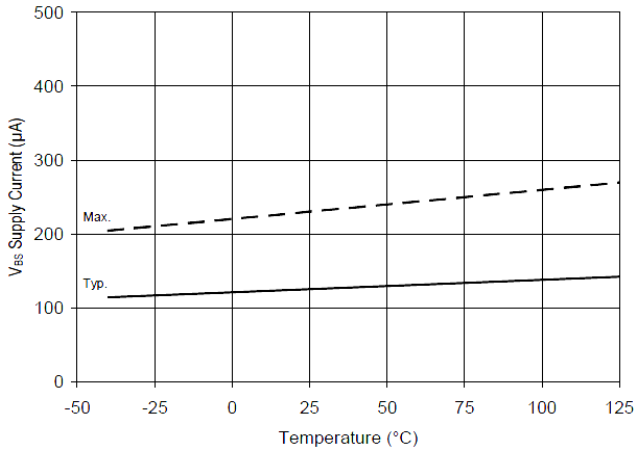


Figure 14A. V_{BS} Supply Current vs. Temperature

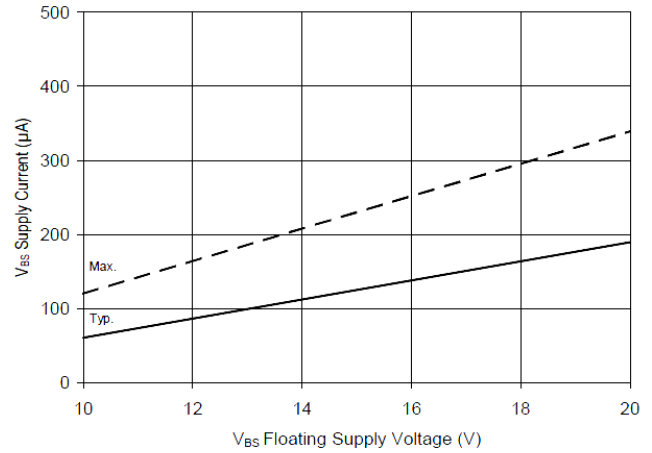


Figure 14B. V_{BS} Supply Current vs. Voltage

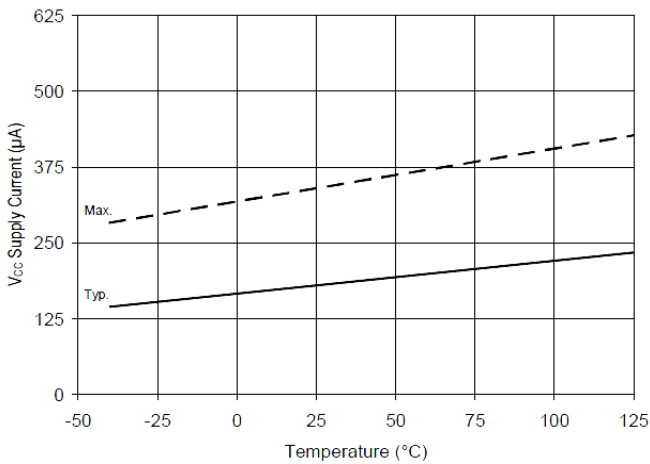


Figure 15A. V_{CC} Supply Current vs. Temperature

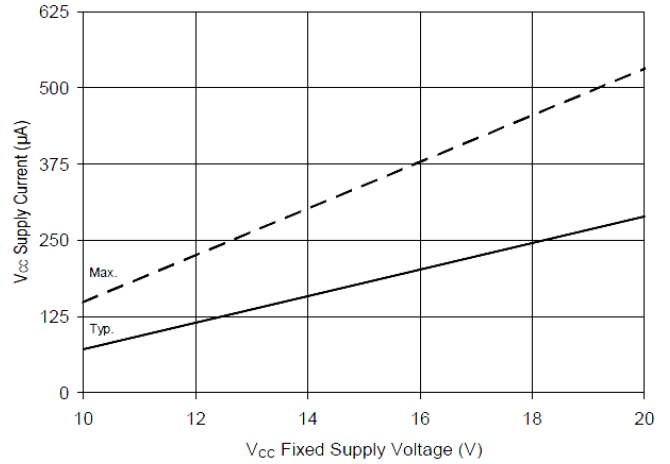


Figure 15B. V_{CC} Supply Current vs. Voltage

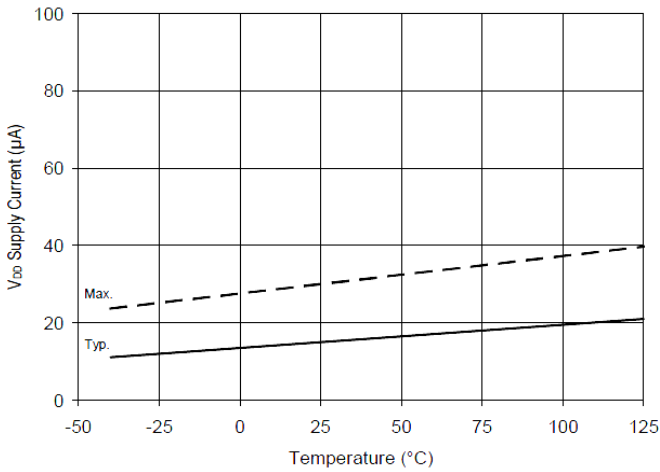


Figure 16A. V_{DD} Supply Current vs. Temperature

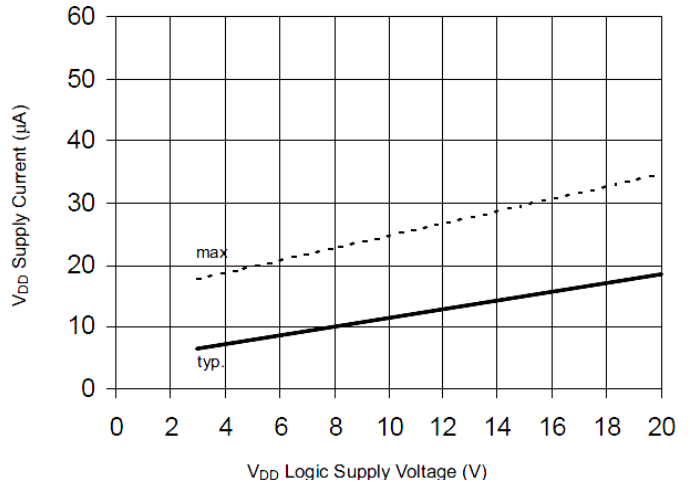


Figure 16B. V_{DD} Supply Current vs. V_{DD} Voltage

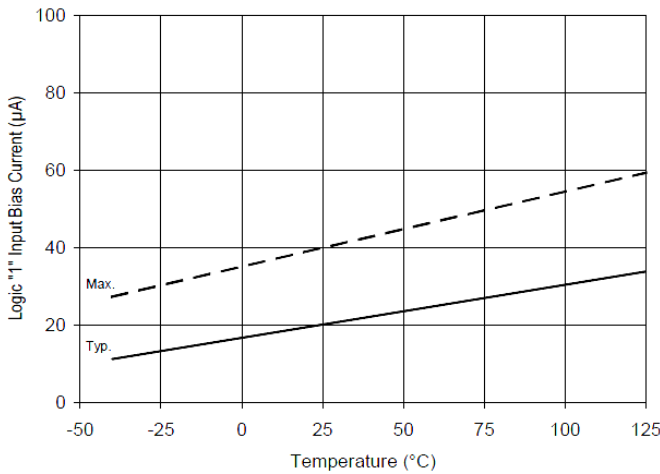


Figure 17A. Logic "1" Input Current vs. Temperature

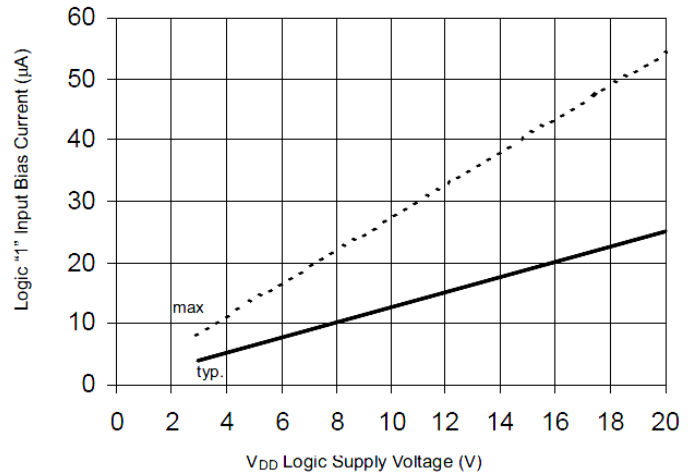


Figure 17B. Logic "1" Input Current vs. V_{DD} Voltage

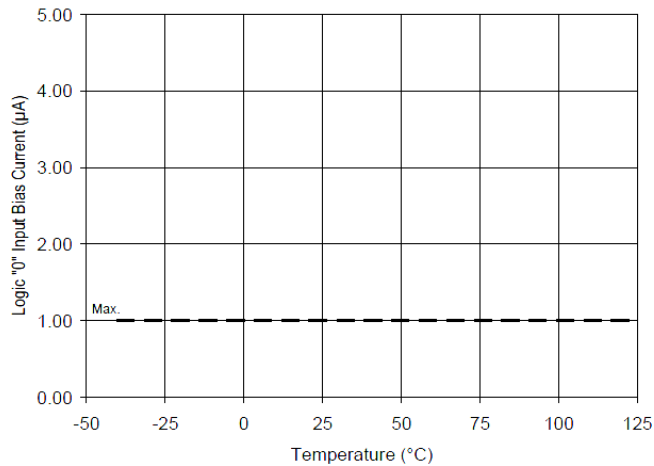


Figure 18A. Logic "0" Input Current vs. Temperature

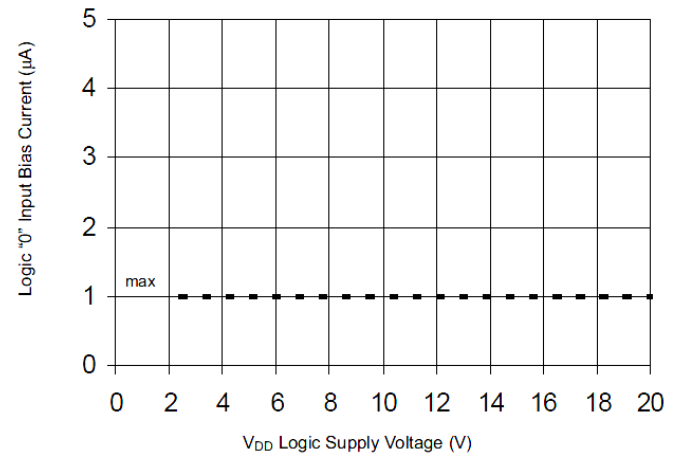


Figure 18B. Logic "0" Input Current vs. V_{DD} Voltage

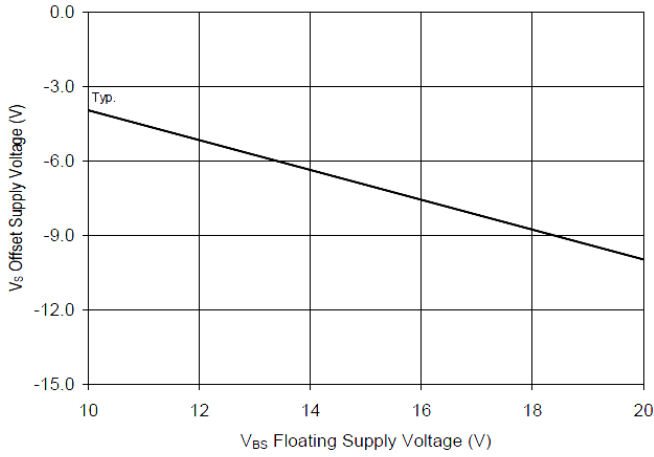


Figure 19. Maximum V_S Negative Offset vs. V_{BS} Supply Voltage

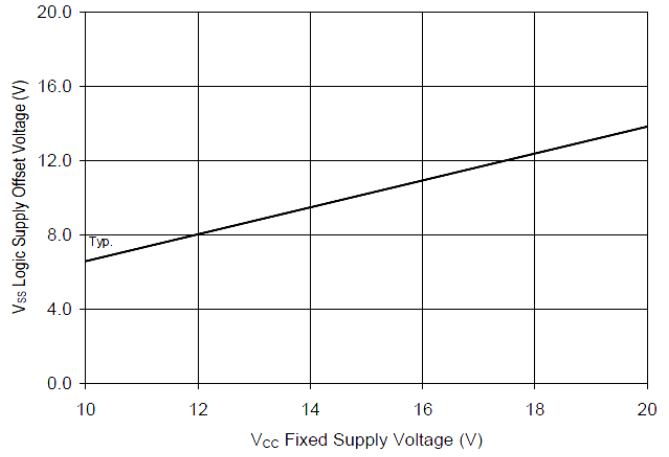
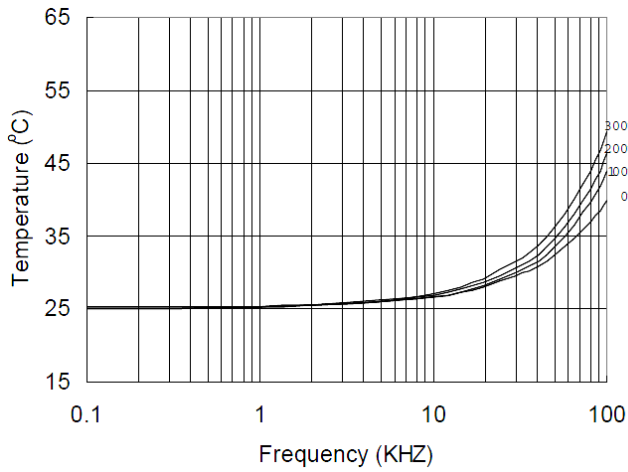
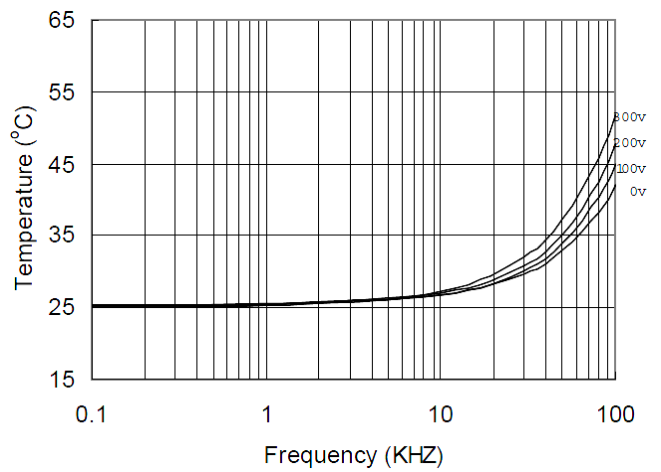


Figure 20. Maximum V_{SS} Positive Offset vs. V_{CC} Supply Voltage



**Figure 21. IR2213S vs. Frequency (IRFBC20)
 $R_{gate}=33\Omega$, $V_{CC}=15V$**



**Figure 22. IR2213S vs. Frequency (IRFBC30)
 $R_{gate}=22\Omega$, $V_{CC}=15V$**

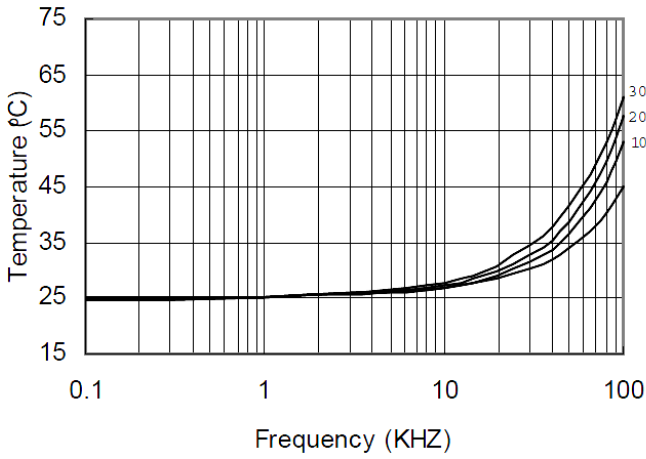


Figure 23. IR2213S vs. Frequency (IRFBC40)
 $R_{gate}=15\Omega, V_{CC}=15V$

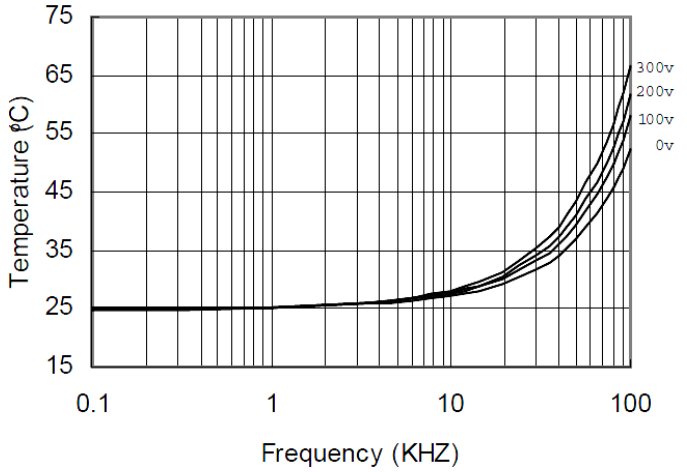


Figure 24. IR2213S vs. Frequency (IRFBC50)
 $R_{gate}=10\Omega, V_{CC}=15V$

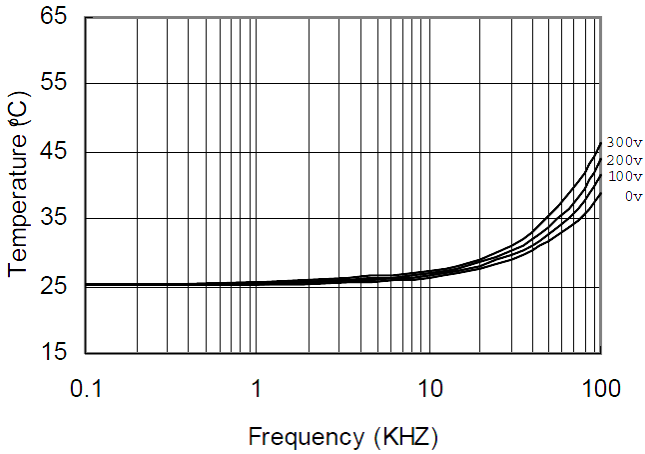


Figure 25. IR2213 vs. Frequency (IRFBC20)
 $R_{gate}=33\Omega, V_{CC}=15V$

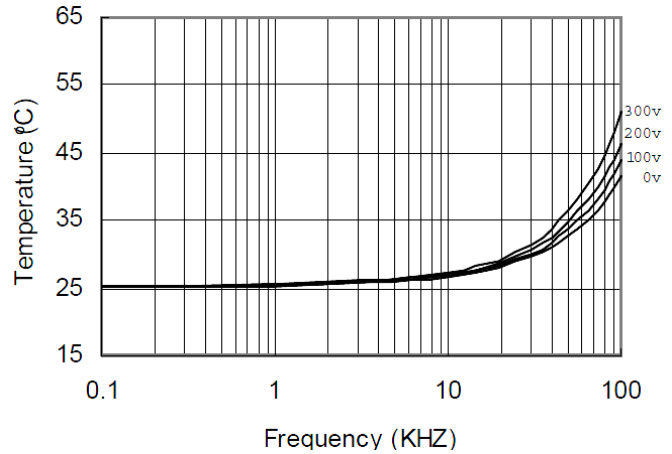


Figure 26. IR2213 vs. Frequency (IRFBC30)
 $R_{gate}=22\Omega, V_{CC}=15V$

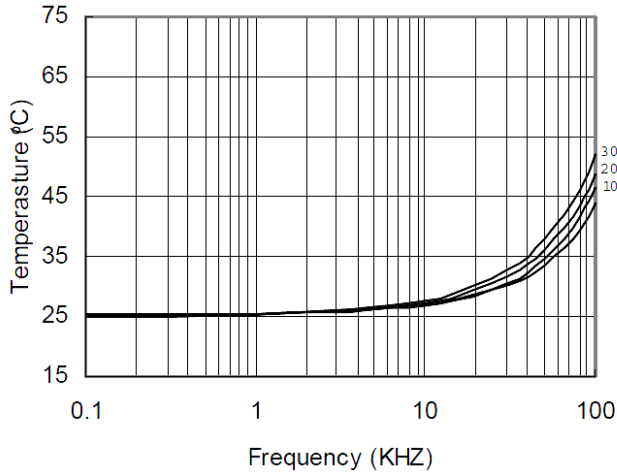


Figure 27. IR2213 vs. Frequency (IRFBC40)
 $R_{gate}=15\Omega, V_{CC}=15V$

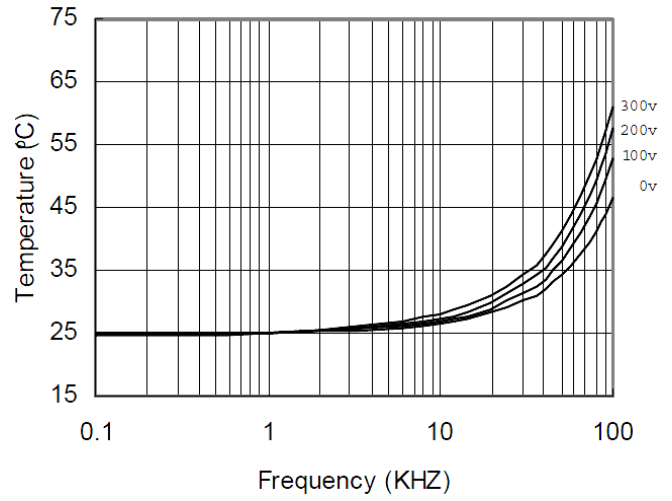
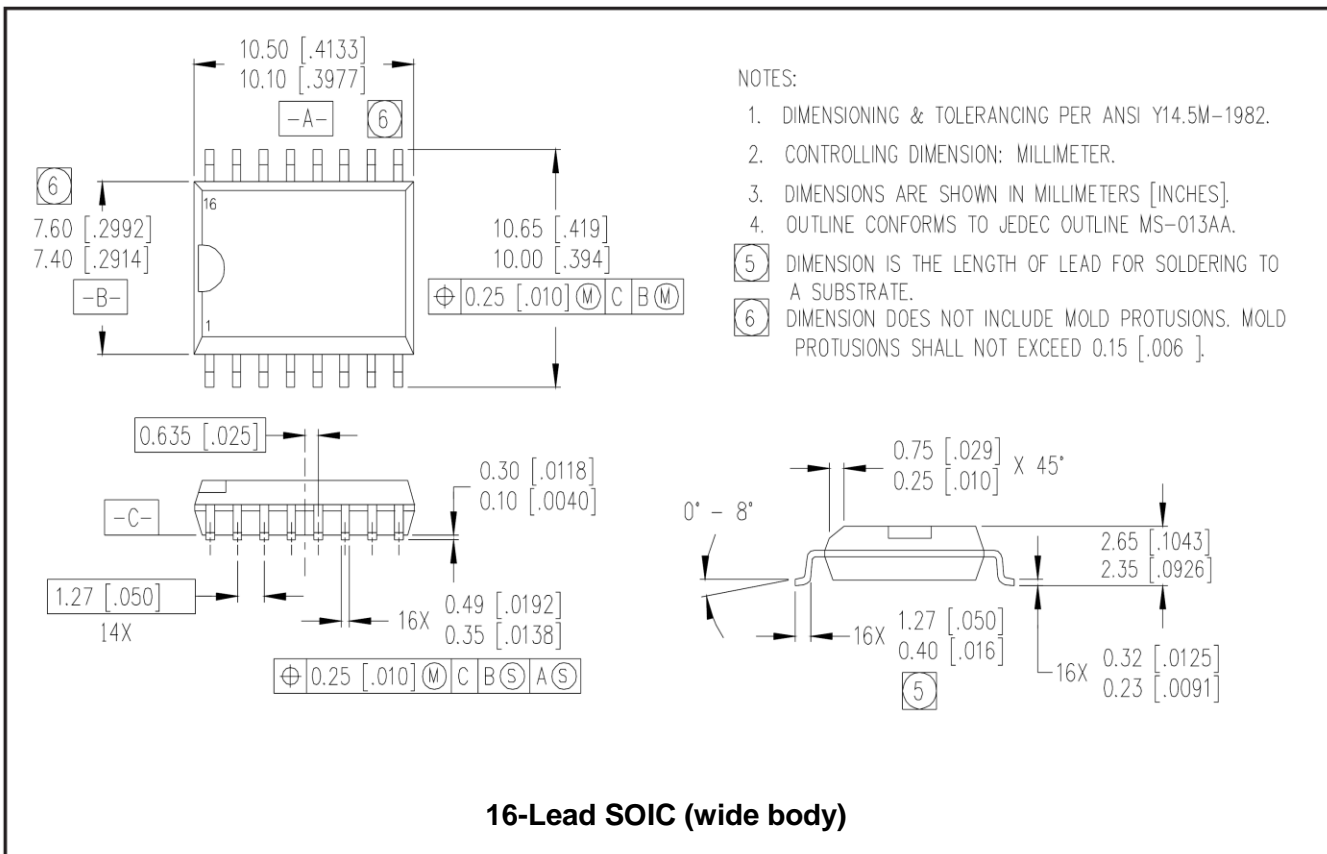
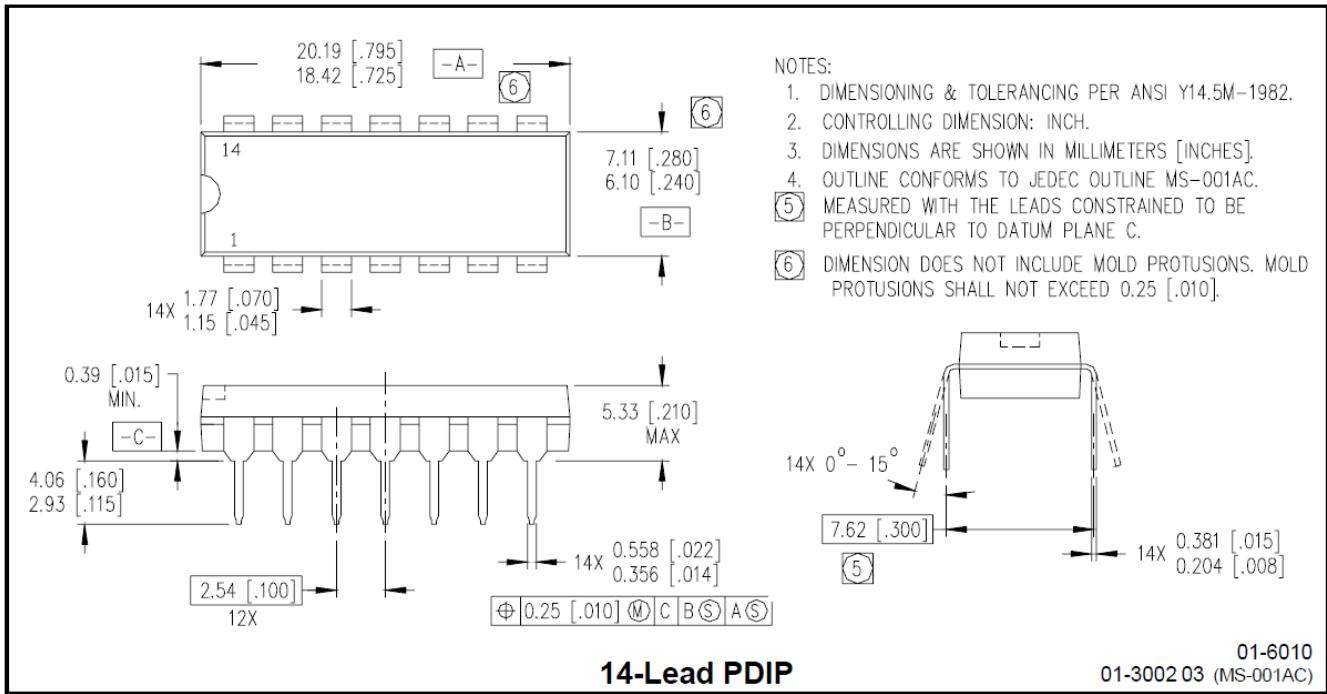
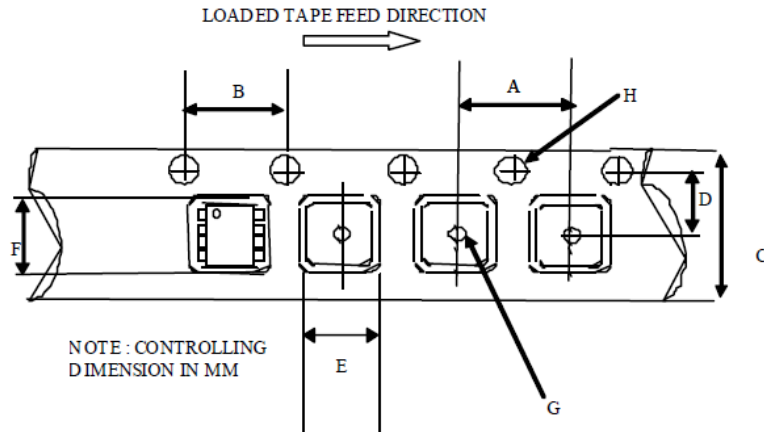
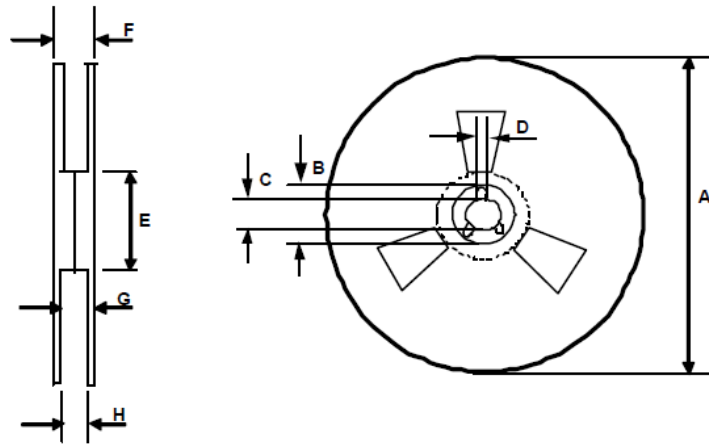


Figure 28. IR2213 vs. Frequency (IRFBC50)
 $R_{gate}=10\Omega, V_{CC}=15V$

Package Details


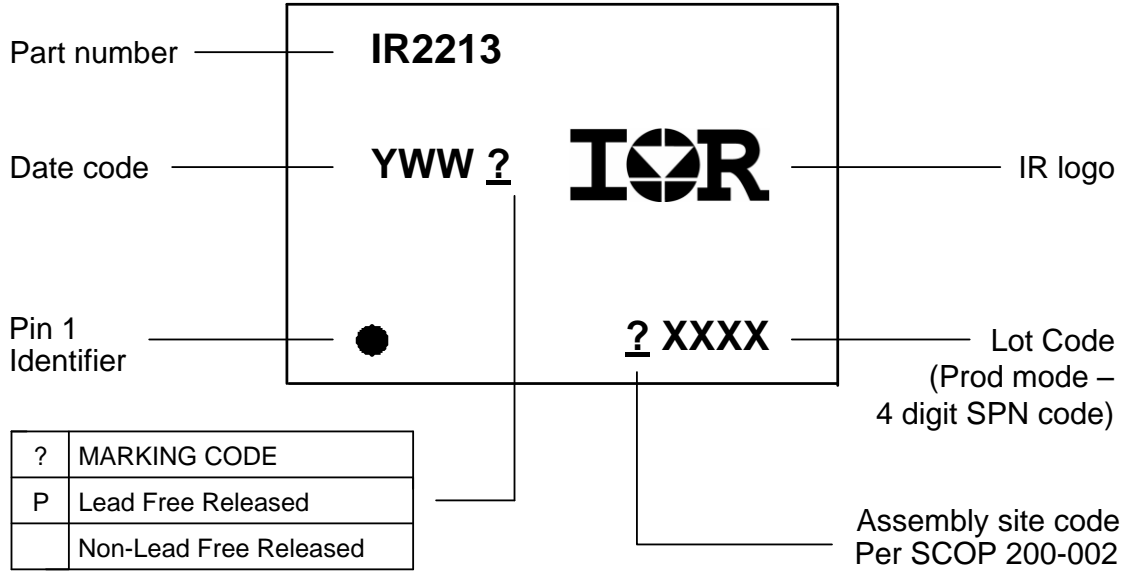
Tape and Reel Details, SO16WB

CARRIER TAPE DIMENSION FOR 16SOICW

| Code | Metric | | Imperial | |
|------|--------|-------|----------|-------|
| | Min | Max | Min | Max |
| A | 11.90 | 12.10 | 0.468 | 0.476 |
| B | 3.90 | 4.10 | 0.153 | 0.161 |
| C | 15.70 | 16.30 | 0.618 | 0.641 |
| D | 7.40 | 7.60 | 0.291 | 0.299 |
| E | 10.80 | 11.00 | 0.425 | 0.433 |
| F | 10.60 | 10.80 | 0.417 | 0.425 |
| G | 1.50 | n/a | 0.059 | n/a |
| H | 1.50 | 1.60 | 0.059 | 0.062 |

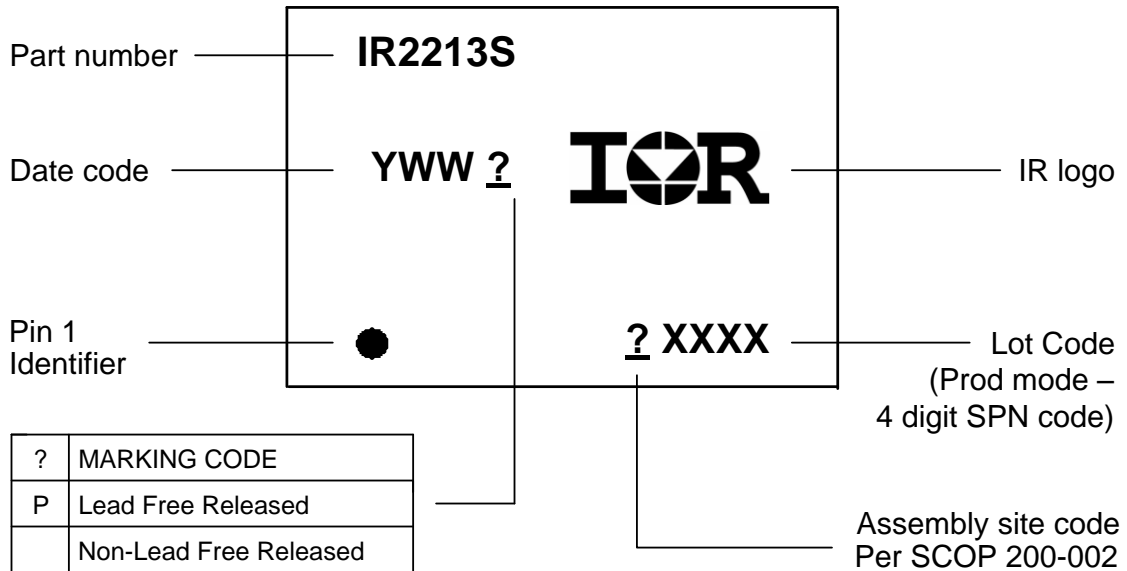

REEL DIMENSIONS FOR 16SOICW

| Code | Metric | | Imperial | |
|------|--------|--------|----------|--------|
| | Min | Max | Min | Max |
| A | 329.60 | 330.25 | 12.976 | 13.001 |
| B | 20.95 | 21.45 | 0.824 | 0.844 |
| C | 12.80 | 13.20 | 0.503 | 0.519 |
| D | 1.95 | 2.45 | 0.767 | 0.096 |
| E | 98.00 | 102.00 | 3.858 | 4.015 |
| F | n/a | 22.40 | n/a | 0.881 |
| G | 18.50 | 21.10 | 0.728 | 0.830 |
| H | 16.40 | 18.40 | 0.645 | 0.724 |

Part Marking Information



14-Lead PDIP



16-Lead SOIC (wide body)

Qualification Information[†]

| | | |
|-----------------------------------|---|---|
| Qualification Level | Industrial ^{††} (per JEDEC JESD 47) | |
| | Comments: This family of ICs has passed JEDEC's Industrial qualification. IR's Consumer qualification level is granted by extension of the higher Industrial level. | |
| Moisture Sensitivity Level | SOIC16WB | MSL3 ^{†††} (per IPC/JEDEC J-STD 020) |
| | PDIP14 | Not applicable (non-surface mount package style) |
| RoHS Compliant | Yes | |

- † Qualification standards can be found at International Rectifier's web site <http://www.irf.com/>
- †† Higher qualification ratings may be available should the user have such requirements. Please contact your International Rectifier sales representative for further information.
- ††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

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For technical support, please contact IR's Technical Assistance Center
<http://www.irf.com/technical-info/>

WORLD HEADQUARTERS:
 233 Kansas St., El Segundo, California 90245
 Tel: (310) 252-7105

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