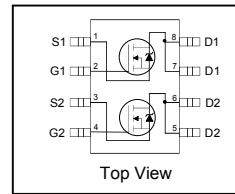


**Features**

- Advanced Planar Technology
- Dual N Channel MOSFET
- Low On-Resistance
- Logic Level Gate Drive
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified \*

**Description**

Specifically designed for Automotive applications, this cellular design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other applications.



$V_{DSS}$	<b>50V</b>
$R_{DS(on)}$ max.	<b>130mΩ</b>
$I_D$	<b>3.0A</b>



<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
AUIRF7103Q	SO-8	Tape and Reel	4000	AUIRF7103QTR

**Absolute Maximum Ratings**

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 4.5\text{V}$	3.0	A
$I_D @ T_A = 70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 4.5\text{V}$	2.5	
$I_{DM}$	Pulsed Drain Current ①	25	
$P_D @ T_A = 25^\circ\text{C}$	Maximum Power Dissipation ③	2.4	W
	Linear Derating Factor	16	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
$E_{AS}$	Single Pulse Avalanche Energy (Thermally Limited) ④	22	mJ
$I_{AR}$	Avalanche Current ①	See Fig.19,20, 16b, 16c	A
$E_{AR}$	Repetitive Avalanche Energy ⑥		mJ
dv/dt	Peak Diode Recovery dv/dt ⑤	12	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	°C

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JL}$	Junction-to-Drain Lead	—	20	°C/W
$R_{\theta JA}$	Junction-to-Ambient ④⑤	—	62.5	

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\*Qualification standards can be found at [www.infineon.com](http://www.infineon.com)

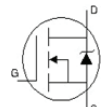
**Static @ T<sub>J</sub> = 25°C (unless otherwise specified)**

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	50	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.057	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	130	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 3.0A ②
		—	—	200		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 1.5A ②
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	—	3.0	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Trans conductance	3.4	—	—	S	V <sub>DS</sub> = 15V, I <sub>D</sub> = 3.0A
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	2.0	μA	V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V
		—	—	25		V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 55°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -20V

**Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

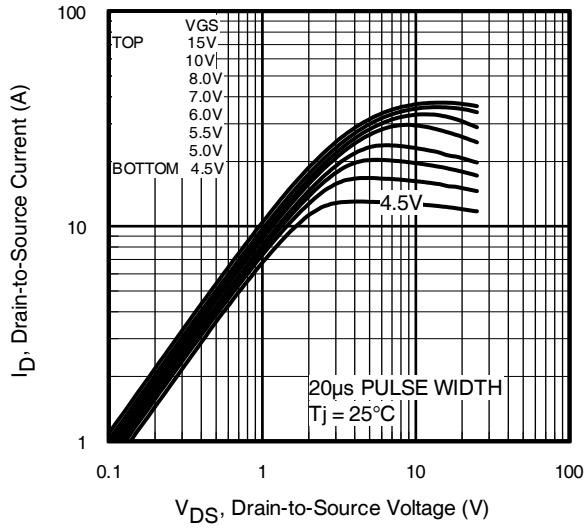
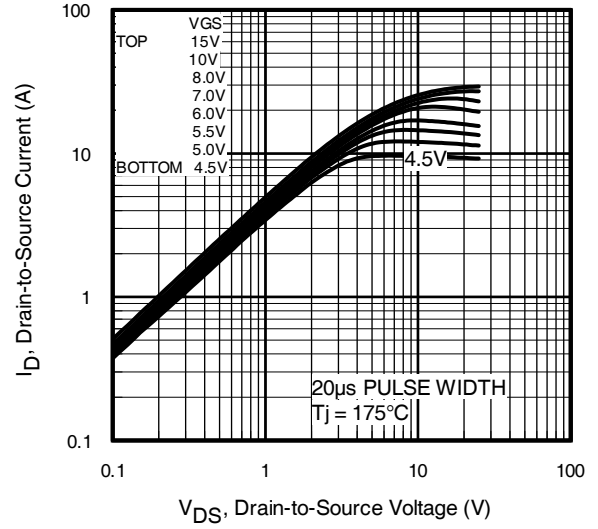
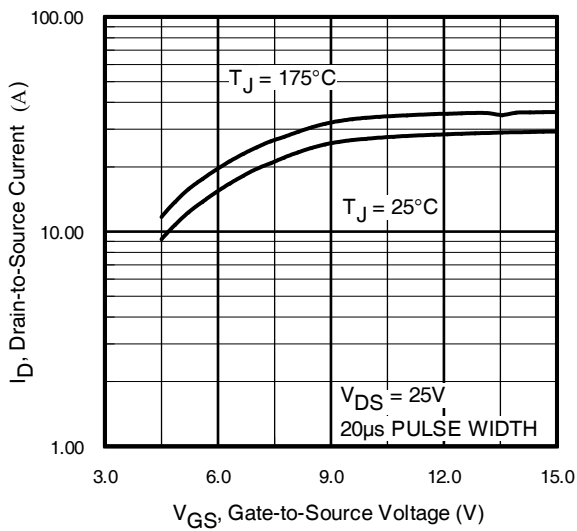
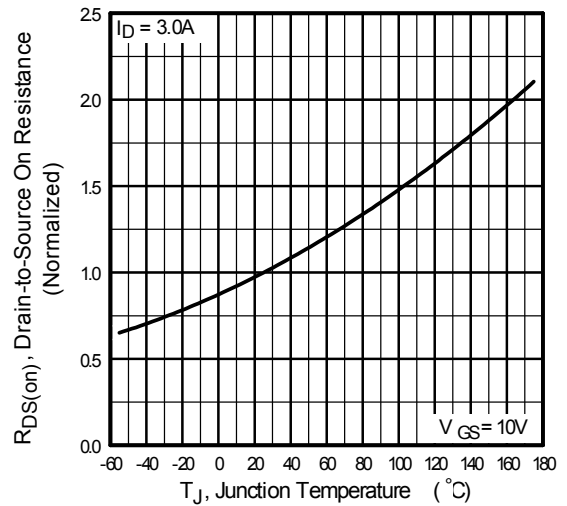
Q <sub>g</sub>	Total Gate Charge	—	10	15	nC	I <sub>D</sub> = 2.0A
Q <sub>gs</sub>	Gate-to-Source Charge	—	1.2	—		V <sub>DS</sub> = 40V
Q <sub>gd</sub>	Gate-to-Drain Charge	—	2.8	—		V <sub>GS</sub> = 10V
t <sub>d(on)</sub>	Turn-On Delay Time	—	5.1	—	ns	V <sub>DD</sub> = 25V
t <sub>r</sub>	Rise Time	—	1.7	—		I <sub>D</sub> = 1.0A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	15	—		R <sub>G</sub> = 6.0Ω
t <sub>f</sub>	Fall Time	—	2.3	—		R <sub>D</sub> = 25Ω ②
C <sub>iss</sub>	Input Capacitance	—	255	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	69	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	29	—		f = 1.0MHz

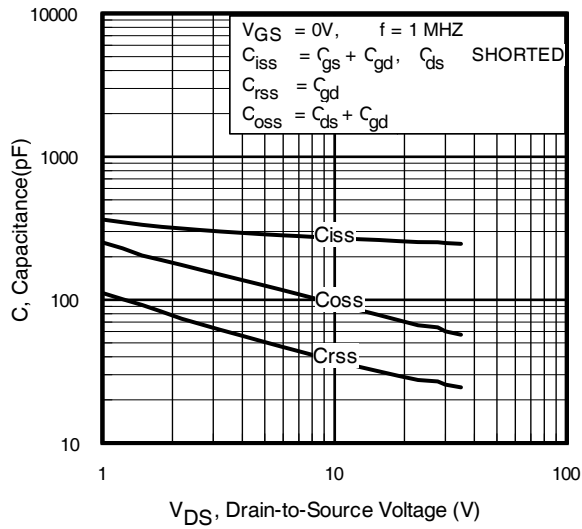
**Diode Characteristics**

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	3.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	12		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.2	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 1.5A, V <sub>GS</sub> = 0V ②
t <sub>rr</sub>	Reverse Recovery Time	—	35	53	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 1.5A,
Q <sub>rr</sub>	Reverse Recovery Charge	—	45	67	nC	di/dt = 100A/μs ②
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

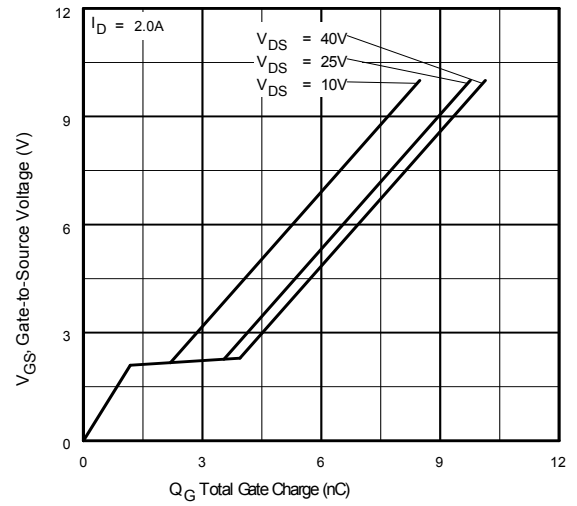
**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ③ Surface mounted on 1" in square Cu board.
- ④ Starting T<sub>J</sub> = 25°C, L = 4.9mH, R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 3.0A. (See Fig. 12)
- ⑤ I<sub>SD</sub> ≤ 2.0A, di/dt ≤ 155A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>J</sub> ≤ 175°C.
- ⑥ Limited by T<sub>Jmax</sub>, see Fig.16b, 16c, 19, 20 for typical repetitive avalanche performance.

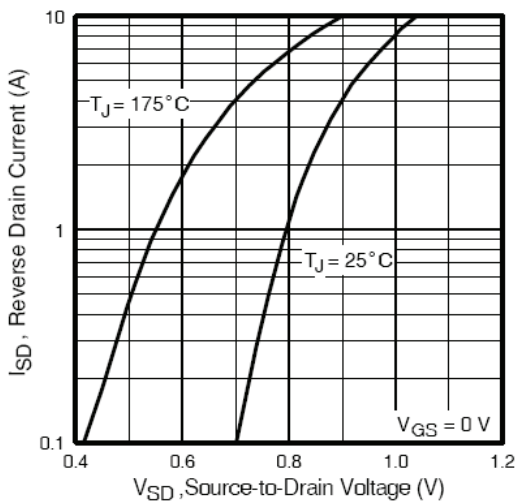

**Fig. 1** Typical Output Characteristics

**Fig. 2** Typical Output Characteristics

**Fig. 3** Typical Transfer Characteristics

**Fig. 4** Normalized On-Resistance vs. Temperature



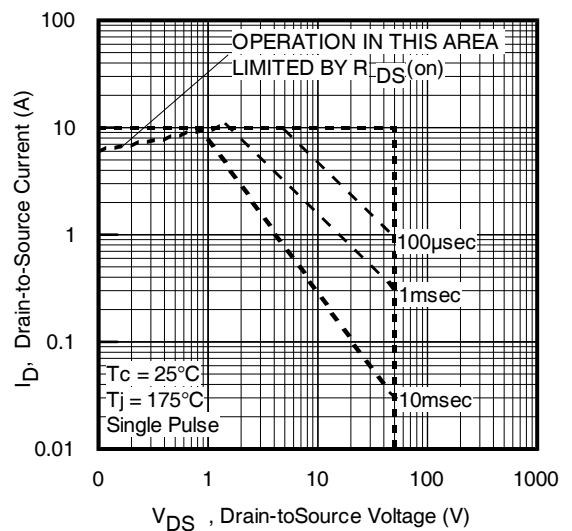
**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



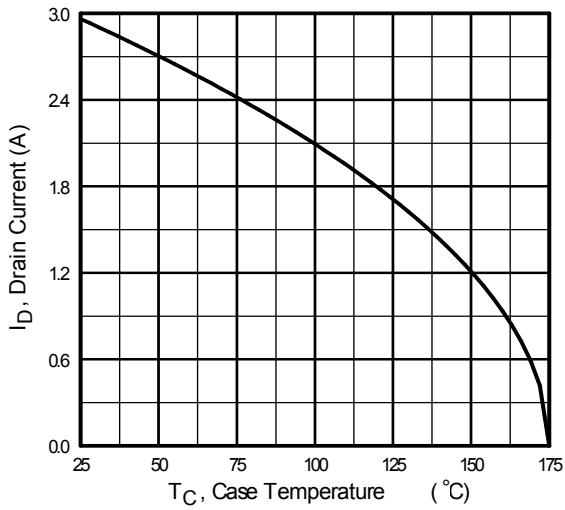
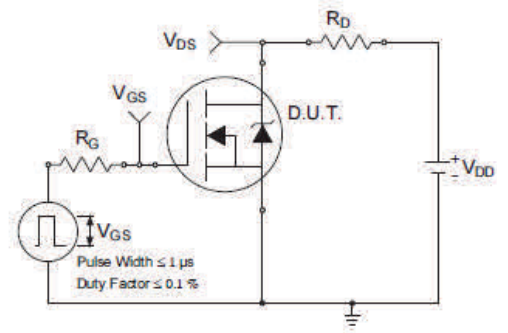
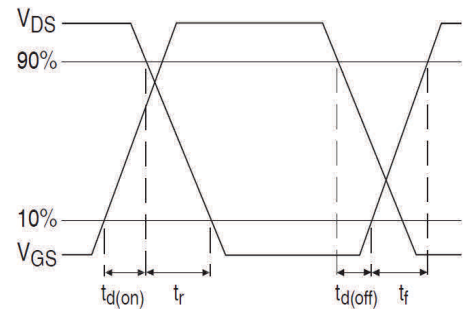
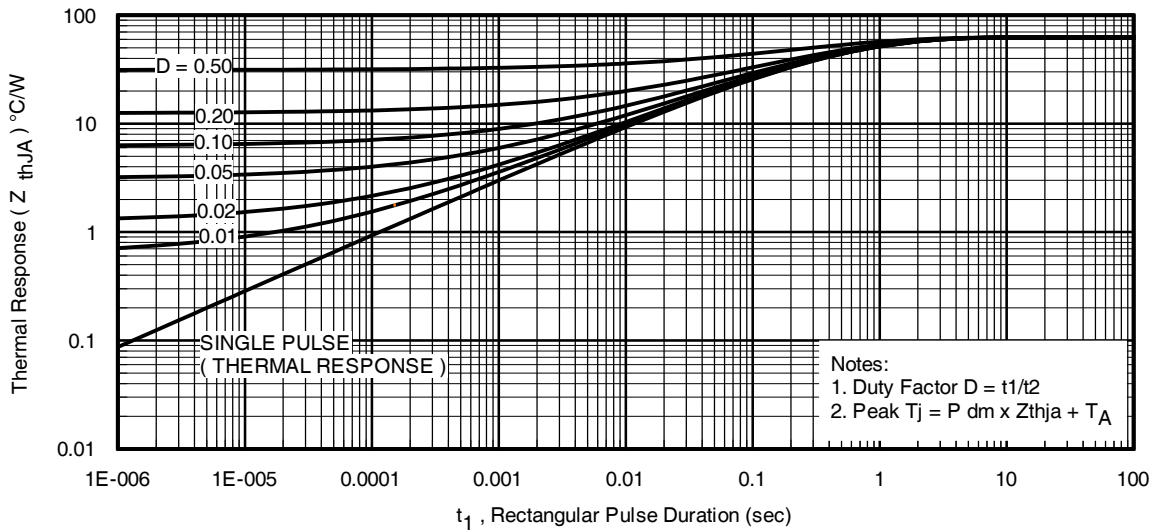
**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

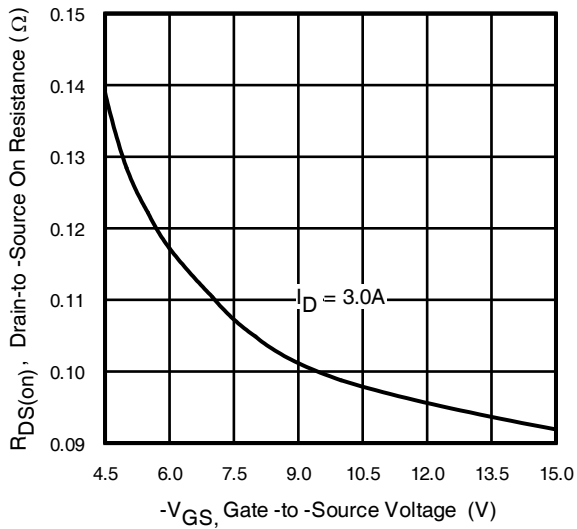


**Fig. 7** Typical Source-to-Drain Diode Forward Voltage

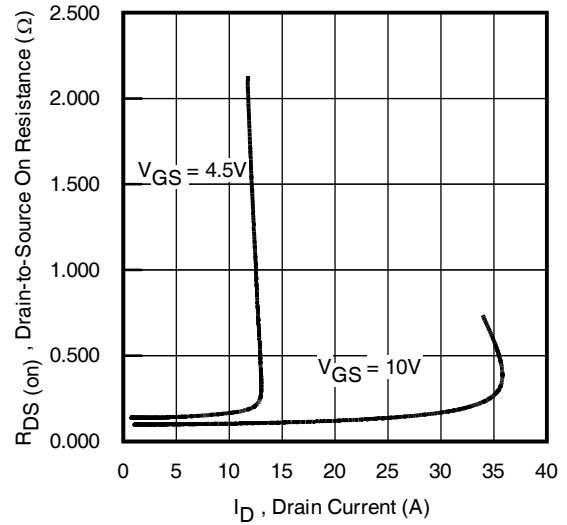


**Fig 8.** Maximum Safe Operating Area

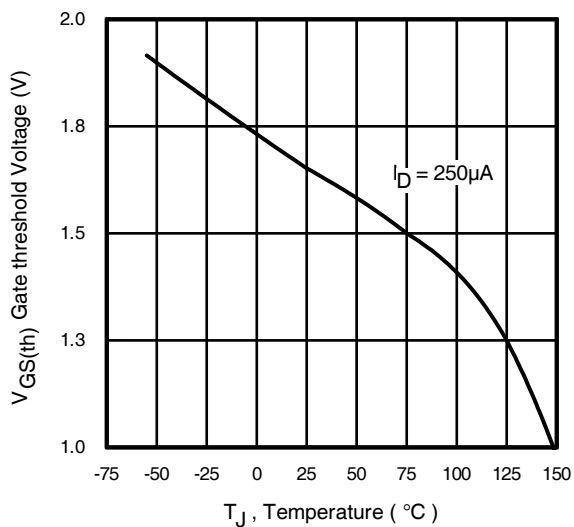

**Fig 9.** Maximum Drain Current vs. Case Temperature

**Fig 10a.** Switching Time Test Circuit

**Fig 10b.** Switching Time Waveforms

**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



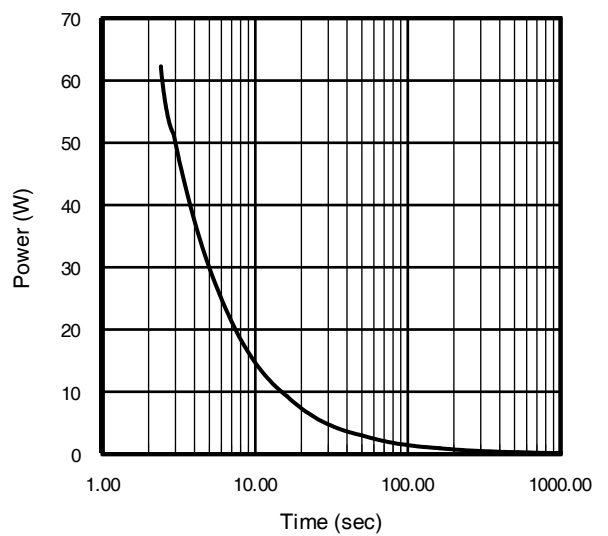
**Fig 12.** Typical On-Resistance Vs. Gate Voltage



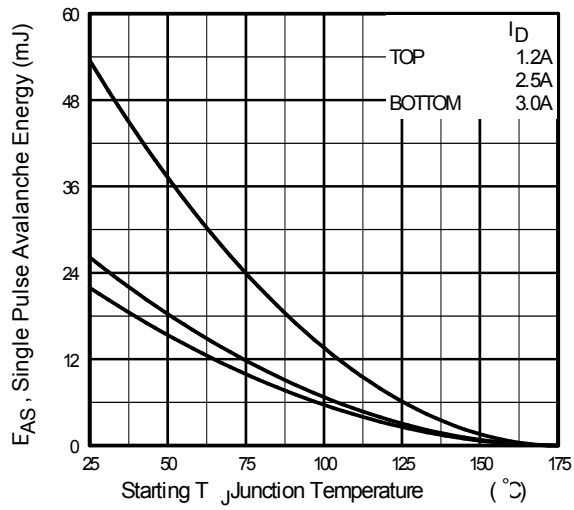
**Fig 13.** Typical On-Resistance Vs. Drain Current



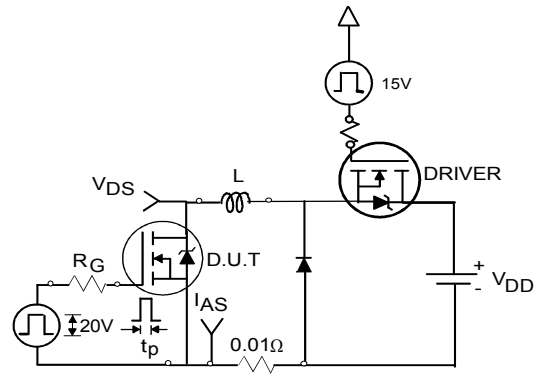
**Fig. 14.** Typical Threshold Voltage Vs. Junction Temperature



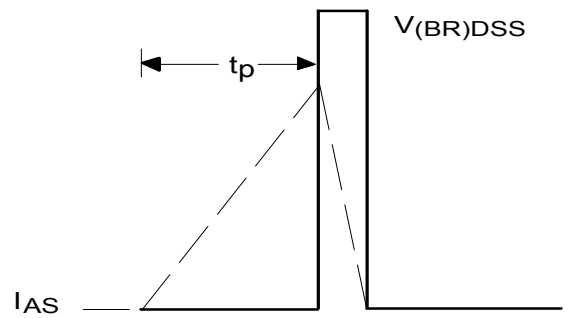
**Fig 15.** Typical Power Vs. Time



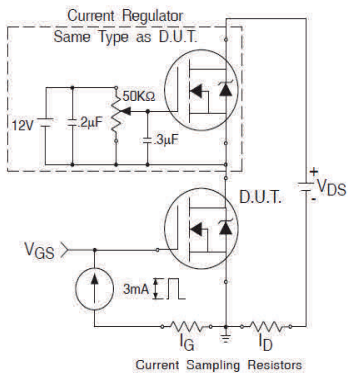
**Fig 16a.** Maximum Avalanche Energy vs. Drain Current



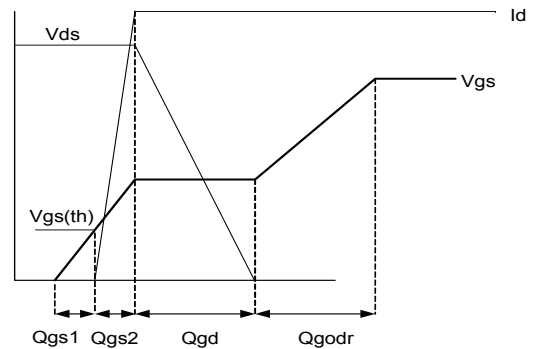
**Fig 16b.** Unclamped Inductive Test Circuit



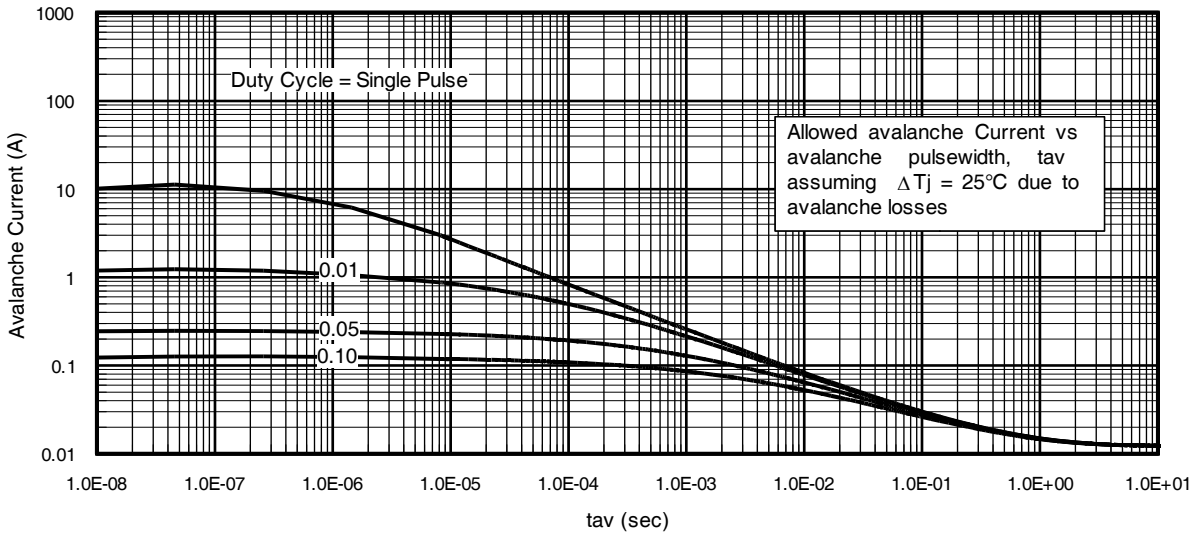
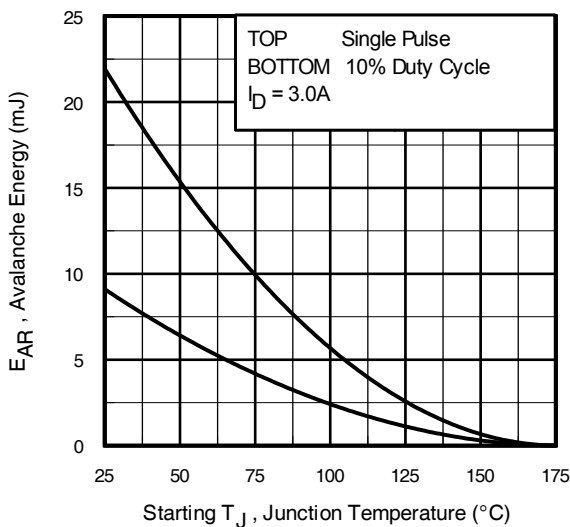
**Fig 16c.** Unclamped Inductive Waveforms



**Fig 17.** Gate Charge Test Circuit



**Fig 18.** Basic Gate Charge Waveform


**Fig 19. Typical Avalanche Current vs. Pulse width**

**Fig 20. Maximum Avalanche Energy vs. Temperature**
**Notes on Repetitive Avalanche Curves , Figures 19, 20:  
(For further info, see AN-1005 at [www.infineon.com](http://www.infineon.com))**

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 16b, 16c.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 11, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 11)

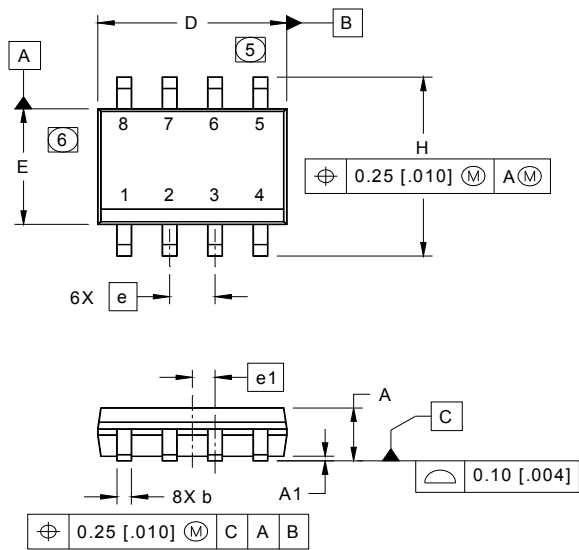
$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [ 1.3 \cdot BV \cdot Z_{thJC} ]$$

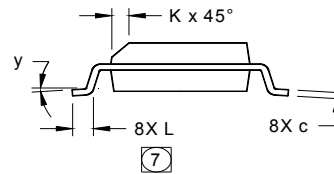
$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



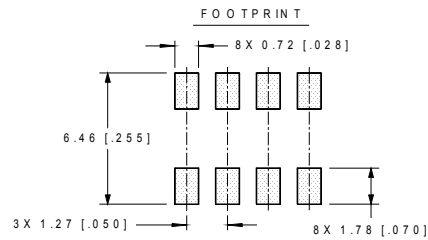
## SO-8 Package Outline (Dimensions are shown in millimeters (inches))



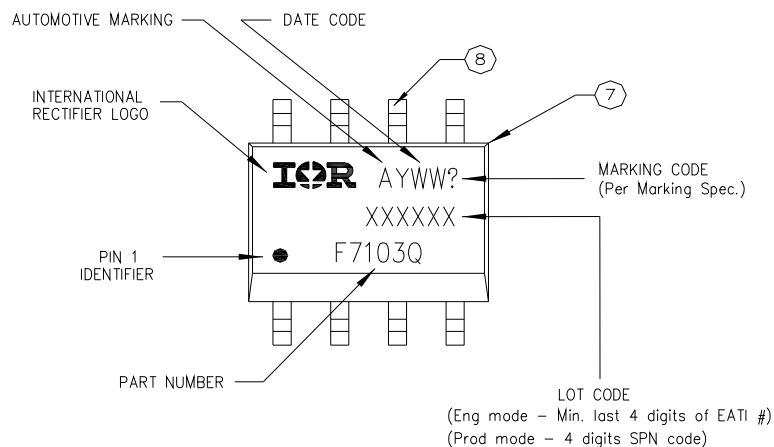
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

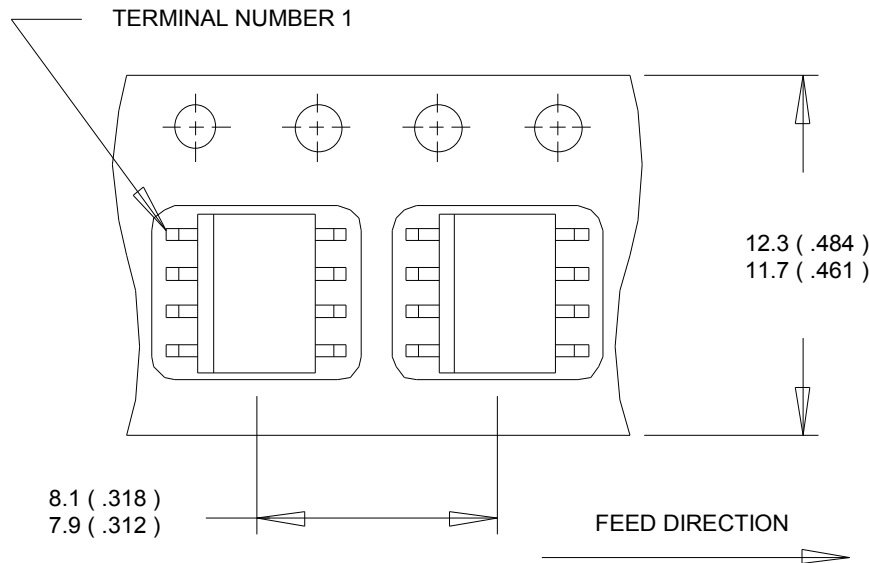


- NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
  2. CONTROLLING DIMENSION: MILLIMETER
  3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
  4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
  5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [0.006].
  6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [0.010].
  7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

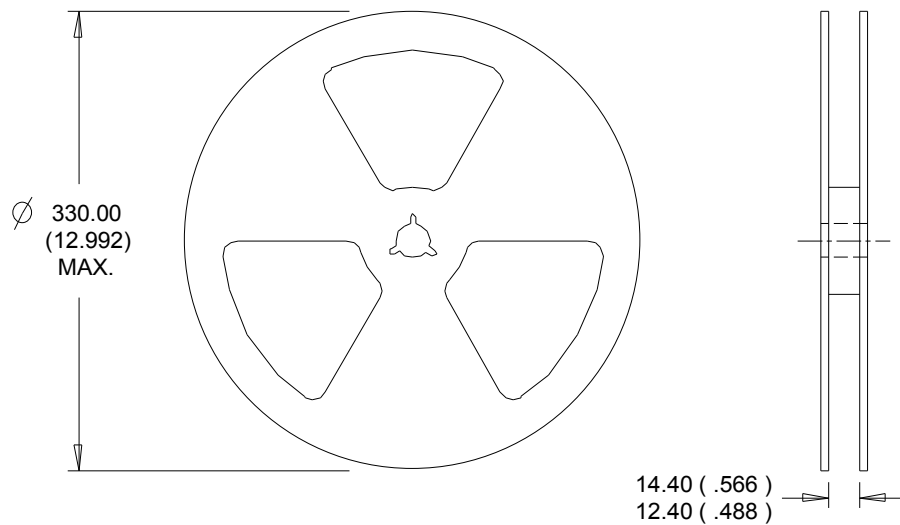


## SO-8 Part Marking Information



**SO-8 Tape and Reel** (Dimensions are shown in millimeters (inches))

**NOTES:**

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.


**NOTES :**

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

**Qualification Information**

<b>Qualification Level</b>		Automotive (per AEC-Q101)	
		Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
<b>Moisture Sensitivity Level</b>		SO-8	MSL1
<b>ESD</b>	Machine Model	Class M1A (+/- 50V) <sup>†</sup> AEC-Q101-002	
	Human Body Model	Class H0 (+/- 250V) <sup>†</sup> AEC-Q101-001	
	Charged Device Model	Class C5 (+/- 1125V) <sup>†</sup> AEC-Q101-005	
<b>RoHS Compliant</b>		Yes	

† Highest passing voltage.

**Revision History**

Date	Comments
4/3/2014	<ul style="list-style-type: none"> <li>Added "Logic Level Gate Drive" bullet in the features section on page 1</li> <li>Updated data sheet with new IR corporate template</li> </ul>
9/30/2015	<ul style="list-style-type: none"> <li>Updated datasheet with corporate template</li> <li>Corrected ordering table on page 1.</li> </ul>

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