IR5001S & (PbF)

UNIVERSAL ACTIVE ORING CONTROLLER

DESCRIPTION

The IR5001S is a universal high-speed controller and N-channel power MOSFET driver for Active ORing and reverse polarity protection applications. The output voltage of the IR5001S is determined based on the polarity of the voltage difference on its input terminals. In particular, if the current flow through an N-channel ORing FET is from source to drain, the output of the IR5001S will be pulled high to Vcc, thus turning the Active ORing FET on. If the current reverses direction and flows from drain to source (due to a short-circuit failure of the source, for example), the IC will quickly switch the Active ORing FET off. Typical turn-off delay for the IR5001S is only 130nS, which helps to minimize voltage sags on the redundant dc voltage.

Both inputs to the IC (INN and INP) as well as Vline input contain integrated high voltage resistors and internal clamps. This makes the IR5001S suitable for applications at voltages up to 100V, and with a minimum number of external components.

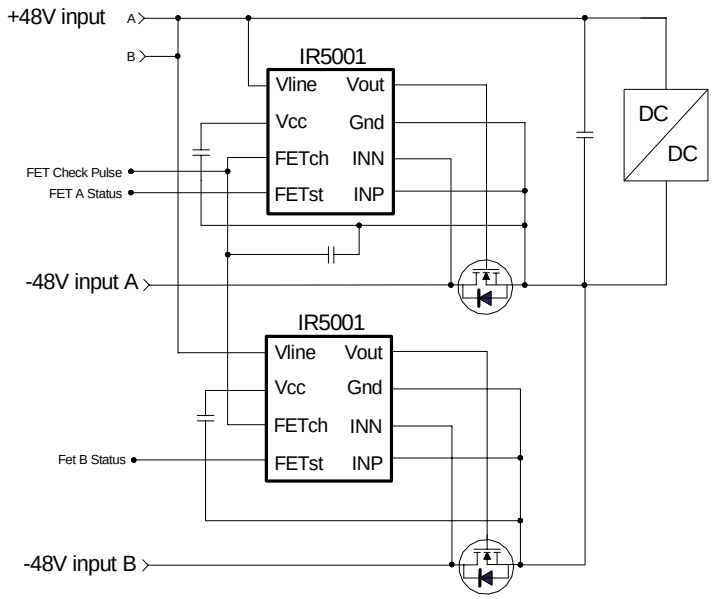
FEATURES

- Controller / driver IC in an SO-8 package for implementation of Active ORing / reverse polarity protection using N-channel Power MOSFETs
- Suitable for both input ORing (for carrier class telecom equipment) as well as output ORing for redundant DC-DC and AC-DC power supplies
- 130ns Typical Turn-Off delay time
- 3A Peak Turn-Off gate drive current
- Asymmetrical offset voltage of the internal high-speed comparator prevents potential oscillations at light load
- Ability to withstand continuous gate short conditions
- Integrated voltage clamps on both comparator inputs allow continuous application of up to 100V
- Option to be powered either directly from 36-75V universal telecom bus (100V max), or from an external bias supply and bias resistor
- Input/Output pins to determine the state of the Active ORing circuit and power system redundancy

APPLICATIONS

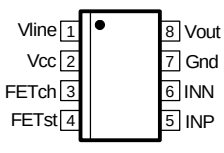
- -48V/-24V Input Active ORing for carrier class communication equipment
- Reverse input polarity protection for DC-DC power supplies
- 24V/48V output active ORing for redundant AC-DC rectifiers
- Low output voltage (12V, 5V, 3.3V...) active ORing for redundant DC-DC and AC-DC power supplies
- Active ORing of multiple voltage regulators for redundant processor power

TYPICAL APPLICATION



F 1 - Typical application of the IR5001S in - 48V input, carrier class telecommunications equipment.

Top View



θ_{JA}=128°C/W

PACKAGE / ORDERING INFORMATION

PKG DESIG.	PART NUMBER	LEADFREE PART NUMBER	PIN COUNT	PARTS PER TUBE	PARTS PER REEL	T & R Oriantation
S	IR5001S	IR5001SPbF	8	95	------	Fig A
S	IR5001STR	IR5001STRPbF	8	-------	2500	

ABSOLUTE MAXIMUM RATINGS

Vline Voltage	-5.0V to 100V (continuous)
Vcc Voltage	-0.5V to 15VDC
Icc Current	5mA
INN, INP Voltage	-5.0V to 100V (continuous)
FETch, FETst	-0.5V to 5.5V
FETst Sink Current	10mA
Junction Temperature	-40°C to 125°C
Storage Temperature Range	-65°C to 150°C

CAUTION:

1. Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied.
2. This device is ESD sensitive. Use of standard ESD handling precautions is required.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, these specifications apply over V_{line} = 36V to 100V; Vcc is decoupled with 0.1uF to Gnd, C_L=10nF at Vout; INP is connected to Gnd. Typical values refer to T_A=25°C. Minimum and maximum limits apply to T_A= 0°C to 85°C temperature range and are 100% production-tested at both temperature extremes. Low duty cycle pulse testing is used which keeps junction and case temperatures equal to the ambient temperature.

PARAMETERS	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Bias Section Vline Bias Current	Iline	Vline=25V	0.14	0.3	0.5	mA
		Vline=36V	0.2	0.5	0.75	
		Vline=100V, Note 1	1.2	1.7	2.2	
VCC output voltage	Vcc(out)	Vline=25V	10.2	12.5	14.1	V
UVLO Section UVLO ON Threshold Voltage	Vcc(ON)	Vline=open, VINP=0; VINN= -0.3V Vcc increased until Vout switches from LO to HI, Note 2	8.0	9.6	10.7	V
UVLO OFF Threshold Voltage	Vcc(OFF)	Vline=open, VINP=0, VINN=-0.3V, Vcc is decreased until Vout switches from HI to LO	5.6	7.2	8.8	
UVLO Hysteresis			1.6	2.3	2.8	V
Input Comparator Section Input Offset Voltage (VINP-VINN)	Vos	VINP=0V and VINN Ramping up, VOUT changes from HI to LO, Fig.3	-7.9	-4.0	0	mV
Input Hysteresis Voltage	Vhyst	VINP=0,VINN ramping down, Figures 3 and 4	13	31	44	
(INN) Input Bias Current	I(INN)	VINP=0V, VINN=36V	0.2	0.5	0.9	mA
(INP) Input Bias Current	I(INP)	VINN=0V, VINP=36V	0.2	0.5	0.9	

PARAMETERS	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Output Section High Level Output Voltage	Vout HI	Vline=25V, IOH=50uA, V(INN)=-0.3V	10.2	11.5	14.1	V
Low Level Output Voltage	Vout LO	IOL=100mA, V(INN)=+0.3V			0.1	V
Turn-On DelayTime	td(on)	Vout switching from LO to HI, Fig.5	5	27	45	us
Rise Time	tr		0.09	0.7	1	ms
Turn-Off Delay Time	td(off)	Vout switching from HI to LO, Fig.5	110	130	170	ns
Fall Time	tf		10	26	39	
FETch and FETst FETch Sink Current	I(FETch)	FETch=5V	-0.5	-1.1	-2	uA
FETch Output Delay Time	FETch_pd	Note 1		0.8	1.8	us
FETch Threshold	Vth(FETch)		0.9	1.2	1.5	V
FETst Threshold Voltage	Vth(FETst)	5k resistor from FETst to 5V logic bias. V(INP) = Gnd, V(INN) ramping down from 0 until FETst switches to Low.	-525	-300	-200	mV
FETst Low Level Output Voltage	VOL	Isink=1mA, V(INN)=-0.5V	0	50	100	mV

Note 1: Guaranteed by design but not tested in production.
Note 2: Low Vcc output voltage corresponds to low UVLO voltage

PIN DESCRIPTIONS

PIN#	PIN SYMBOL	PIN DESCRIPTION
1	Vline	IC power supply pin for 36V to 75V input communications systems. Minimum 25V has to be applied at this pin to bias the IC.
2	Vcc	Output pin of the internal shunt regulator, or input pin for biasing the IC via external resistor. This pin is internally regulated at 12.5V typical. A minimum 0.1uF capacitor must be connected from this pin to Gnd of IR5001.
3	FETch	FET check input pin. Together with FET status output pin, the FETch pin can be used to determine the state of the Active ORing circuit and power system redundancy.
4	FETst	FET status output pin. Together with FETch input pin, the FETst pin can be used to determine the state of the Active ORing circuit and power system redundancy.
5	INP	Positive input of internal comparator. This pin should connect to the source of N-channel Active ORing MOSFET.
6	INN	Negative input pin of internal comparator. This pin should connect to the drain of N-channel Active ORing MOSFET.
7	Gnd	Ground pin of the IR5001.
8	Vout	Output pin for the IR5001. This pin is used to directly drive the gate of the Active Oring N-Channel MOSFET.

BLOCK DIAGRAM

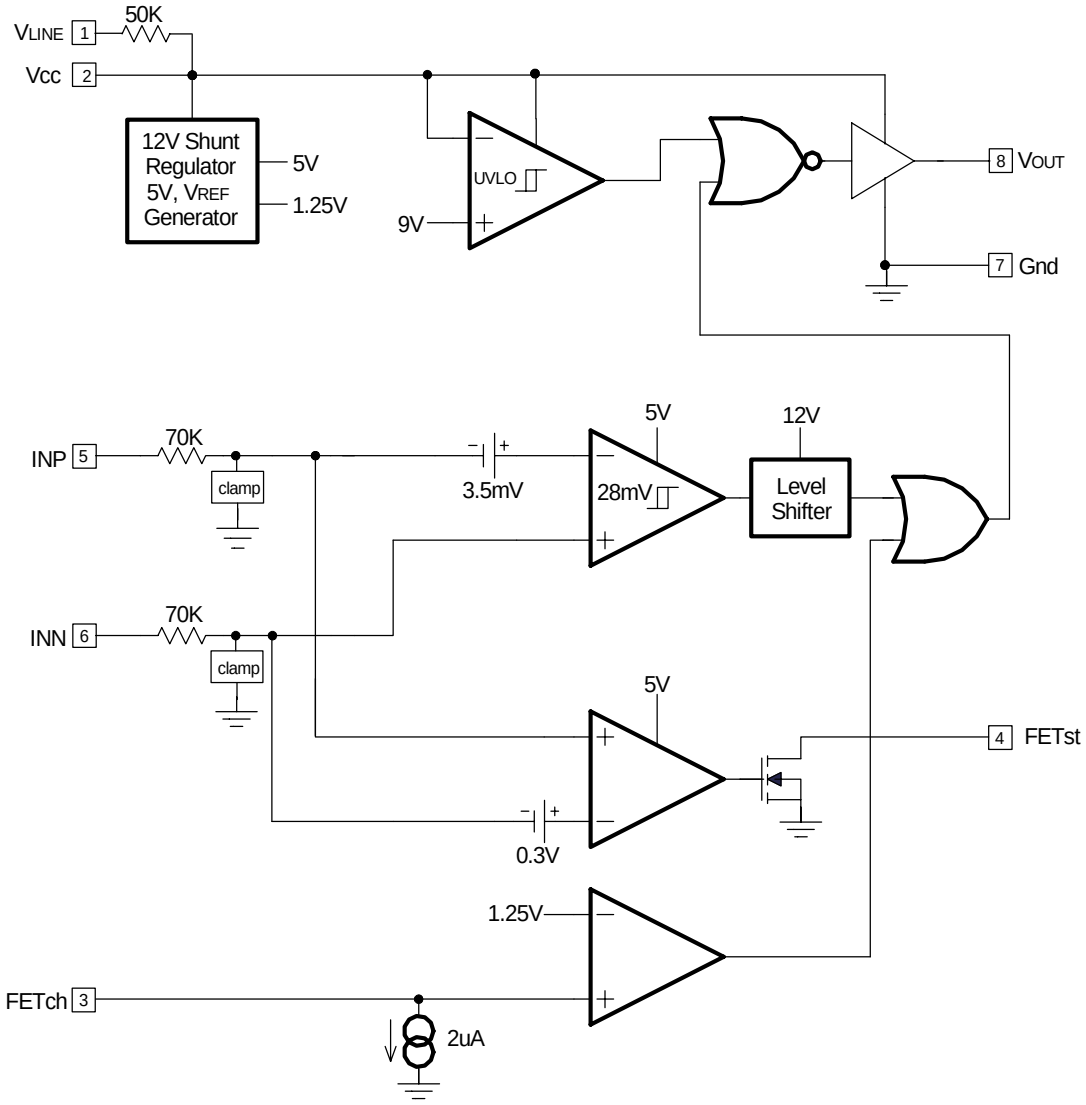


Figure 2 - Simplified block diagram of the IR5001.

PARAMETER DEFINITION AND TIMING DIAGRAM

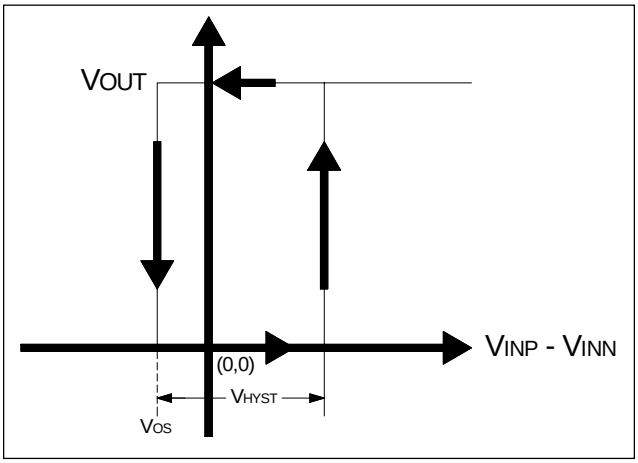


Figure 3 - Input Comparator Offset (Vos) and Hysteresis Voltage (Vhyst) Definition.

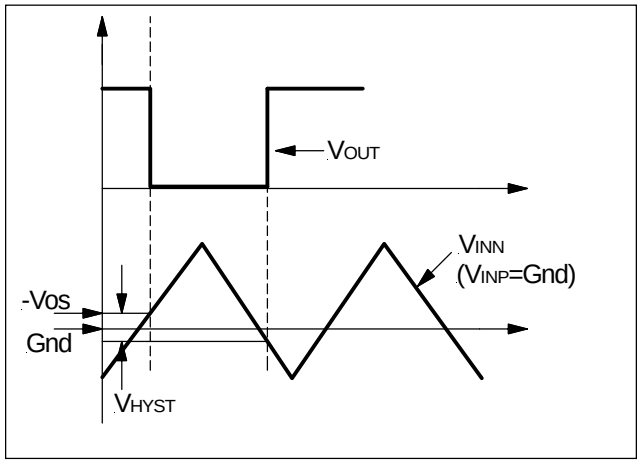


Figure 4 - Input Comparator Hysteresis Definition.

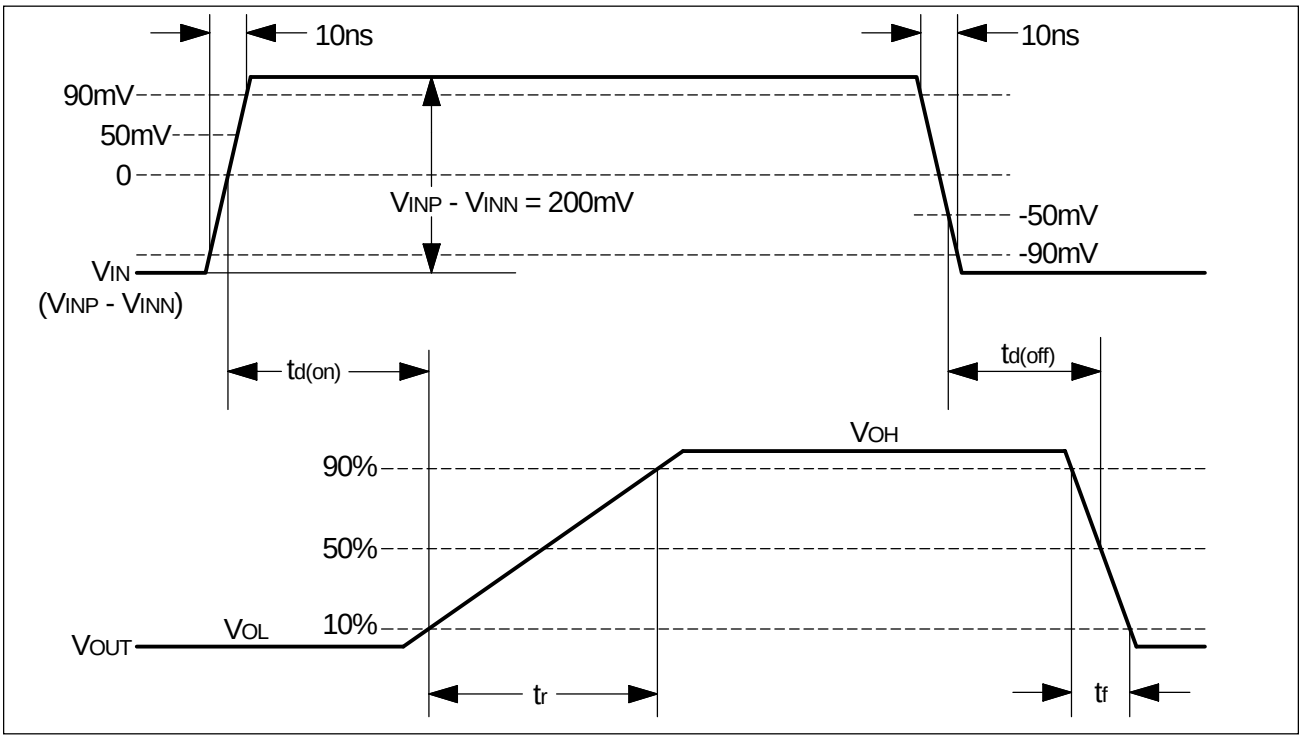


Figure 5 - Dynamic Parameters.

TYPICAL OPERATING CHARACTERISTICS

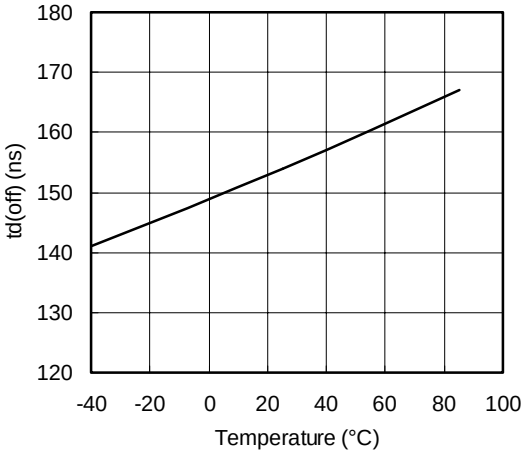


Figure 6 - Turn Off Delay vs. Junction Temperature

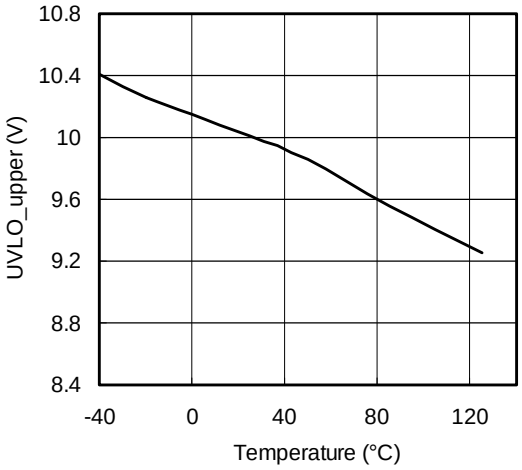


Figure 7 - UVLO Upper Trip Point vs. Junction Temperature

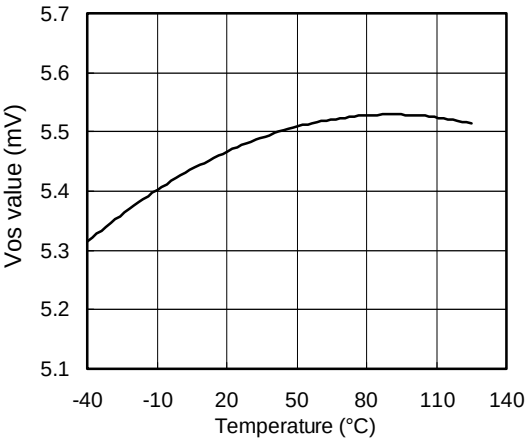


Figure 8 - Vos vs. Junction Temperature

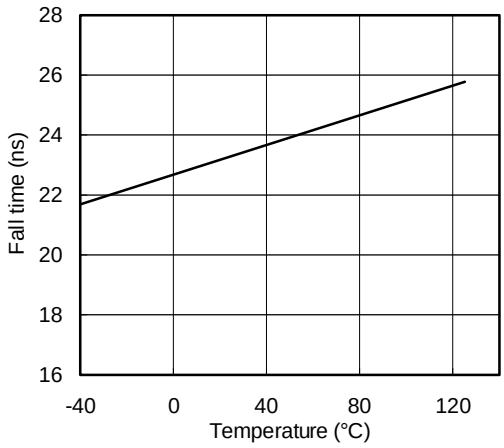


Figure 9 - Fall Time vs. Junction Temperature

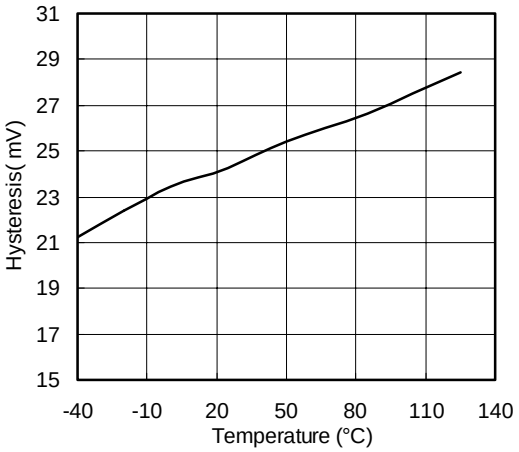


Figure 10 - INP, INN Input Hysteresis vs. Junction Temp.

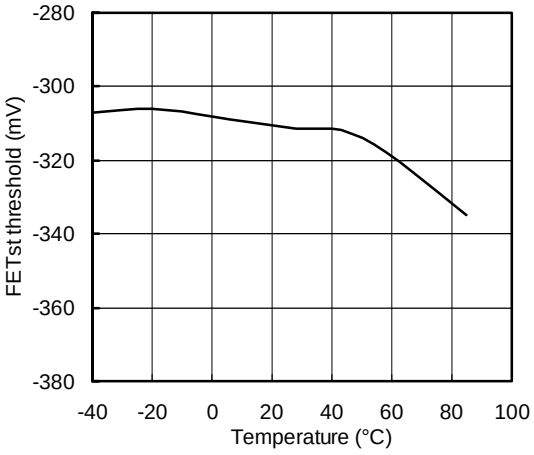


Figure 11 - FETst Threshold Voltage vs. Junction Temp.

TYPICAL OPERATING CHARACTERISTICS

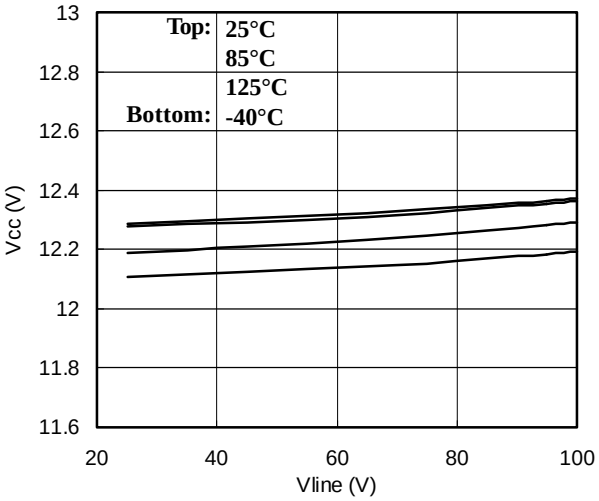


Figure 12 - Vcc vs. Vline and Junction Temperature

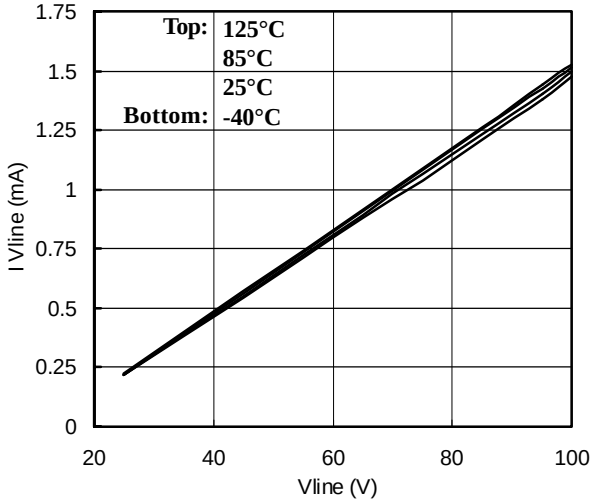


Figure 13 - I(Vline) vs. Vline and Junction Temperature

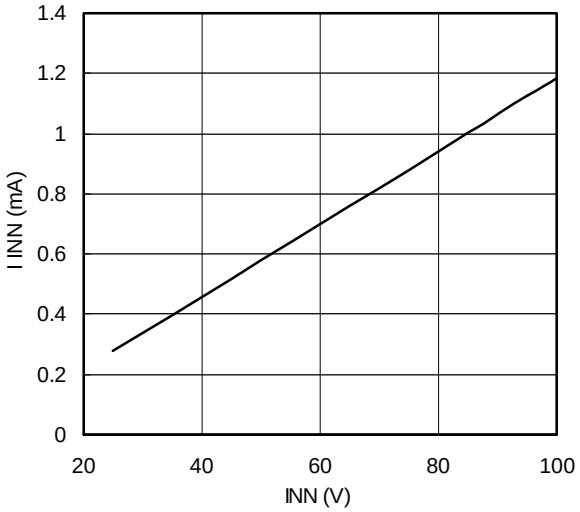


Figure 14 - Bias Current I(INN) vs. V(INN) at Vline=25V

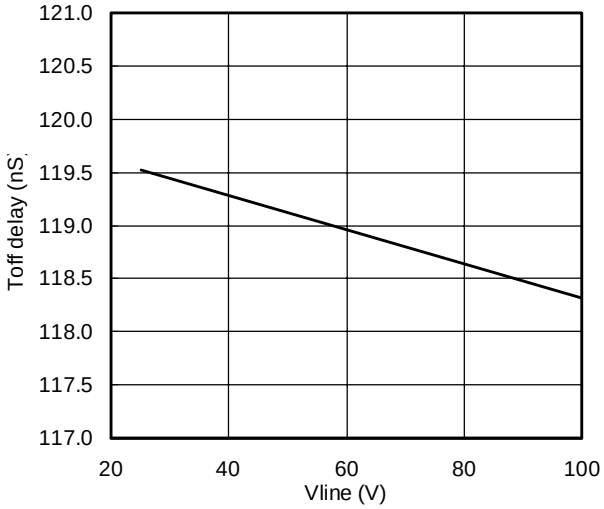


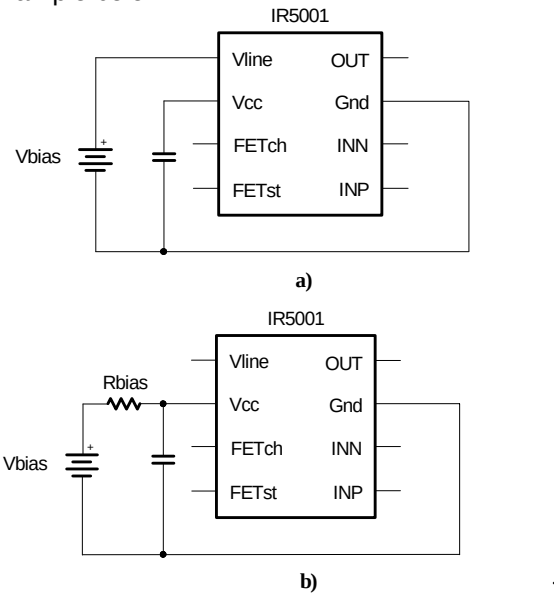
Figure 15 - Turn Off Delay vs. Vline at Room Temperature

DETAILED PIN DESCRIPTION

Vline and Vcc

Vline and Vcc are the input and output pins of the internal shunt regulator. The internal shunt regulator regulates the Vcc voltage at ~12V. The Vcc pin should always be by-passed with a ceramic capacitor to the Gnd pin.

Both Vline and Vcc pins can be used for biasing the IR5001S, as shown in Fig. 16. The Vline pin is designed to bias the IR5001S directly when the available bias voltage is above 25V and less than 100V (targeted at typical 36V – 75V telecom applications). This connection is shown in Fig 16.a. If the available Vbias voltage is lower than 25V, then the IC must be biased using Vcc pin and an external bias resistor as shown in Fig. 16.b. If the available bias voltage is above 100V, both Vline and Vcc pins can be used with an external bias resistor. For calculation of the proper bias resistor value, see example below.



Figue 16 - Biasing options for IR5001

When the Vcc pin is used for biasing the IR5001S, the Vbias must always be higher than the maximum value of the Vcc UVLO threshold (10.7V). The Rbias resistor should always be connected between the Vbias voltage source and Vcc pin. The Rbias resistor is selected to provide adequate Icc current for the IC. The minimum required Icc to guarantee proper IC operation under all conditions is 0.5mA. The maximum Icc is specified at 5mA.

An example of Rbias calculation is given below. Vbias voltages used in the example are referenced to IR5001S Gnd:

Vbias min = 12V
Vbias max = 16V
Rbias = (Vbias min – Vcc UVLOmax) / Icc min =
= (12V – 10.7V) / 0.5mA = 2.6kOhm

Next, using a minimum Vcc (10.2V), verify that Icc with the selected Rbias will be less than 5mA:

Icc max = (Vbias max – Vcc min)/Rbias =
= (16V - 10.2V) / 2.6kOhm = 2.23mA

Since 2.23mA is below 5mA max Icc, the calculated Rbias (2.6kOhm) can be used in this design.

INP and INN Inputs

INP and INN are the inputs of the internal high-speed comparator. Both pins have integrated on-board voltage clamps and high-voltage 70kOhm resistors.

In a typical application, INP should be connected to the source of the N-FET and INN to the drain. To improve the noise immunity, the connections from INN and INP pins to the source and drain terminals of the N-FET should be as short as possible.

The (INP – INN) voltage difference determines the state of the Vout pin of the IR5001S. When the body diode of the Active ORing N-FET is forward-biased and the current first starts flowing, the voltage difference INP – INN will quickly rise toward ~700mV (typical body diode forward voltage drop). As soon as this voltage exceeds Vhyst – $|Vos|$ (27mV typical), the Vout of the IR5001S will be pulled high, turning the channel of the active ORing FET on. As the channel of the N-FET becomes fully enhanced, the (INP – INN) will reduce and stabilize at the value determined by the source-drain current, Isd, and Rds(on) of the N-FET:

(INP – INN) steady state = Isd * $R_{DS(on)}$.

If for some reason (due to a short-circuit failure of the source, for example), the current reverses direction and tries to flow from drain to source, the (INP – INN) will become negative; The IR5001S will then quickly pull its output low, switching the ORing FET off. For considerations regarding the selection of the Active ORing N-FET and $R_{DS(on)}$, see Applications Information Section.

The offset voltage of the internal high-speed comparator is centered around negative 4mV, and is always less than 0mV. This asymmetrical offset

guarantees that once the ORing N-FET is conducting and Vout of the IR5001S is high (FET current flows from source to drain), the current must reverse the direction before the IR5001S will switch the FET off. The asymmetrical offset voltage prevents potential oscillations at light load that could otherwise occur if the offset voltage was centered around 0mV (as is the case in standard comparators).

Vout

Vout is the output pin of the IR5001S, and connects directly to the gate of the external Active ORing N-FET. The voltage level at the Vout pin is typically a diode drop lower than the Vcc voltage.

FETst and FETch

FETch and FETst pins are diagnostic pins that can be used to determine the status of the Active ORing circuit.

FETst is an open-drain output pin. When the voltage difference between VINP - VINN is less than 0.3V, the FETst pin will be logic high. This is normally the case when Active ORing is operating properly (VINP - VINN is less than ~100mV). If the Active ORing FET is not turned on while the IR5001S is properly biased, the output of the FETst pin will be logic low (only the body diode of the N-FET is conducting, and VINP - VINN is ~700mV).

FETch pin. In traditional systems with diode ORing, it is not possible to determine if the diode is functioning properly unless external circuitry is used. For example, the diode could be failed short, and the system would not be aware of it until the source fails and the whole system gets powered down due to lost redundancy (shorted diode failed to isolate the source failure). With the FETch pin it is possible to perform a periodic check of the status of the Active ORing circuit to assure that system redundancy is maintained.

In the IR5001S, the FETch pin is an input pin that can be used to turn off the output of the IR5001S: logic high signal on FETch will pull the Vout pin low, and turn-off the channel of the Active ORing N-FET. This will force the current to flow through the body diode, resulting in VINP – VINN voltage increase from less than ~100mV, to ~700mV. This voltage increase will be reported at FETst pin, which will switch from logic high to logic low, and indicate that the Active ORing circuit is working properly. Failure of the FETst pin output to change from logic high to logic low would indicate that the Active ORing circuit may not be operating as designed, and the system may no longer have power redundancy. For details on how to use this feature consult IR5001S Evaluation Kit, **P/N IRDC5001-LS48V**.

If the FETch pin is not used, it should be tied to ground (for noise immunity purposes). FETst pin should be left open if unused.

Gnd

In typical target applications, the ground pin (Gnd) of IR5001S is connected to the source of the Active ORing N-FET.

APPLICATION INFORMATION

The IR5001S is designed for multiple active ORing and reverse polarity protection applications with minimal number of external components. Examples of typical circuit connections are shown below.

Negative Rail ORing/Reverse Polarity Protection

A typical connection of the IR5001S in negative rail Active ORing or reverse polarity protection is shown in Fig. 17. In this example, IR5001S is biased directly from the positive rail. However, any of the biasing schemes shown in Fig. 16 can be used.

For input ORing in carrier-class communications boards, one IR5001S is used per feed. This is shown in Fig.1. An evaluation kit is available for typical system boards, with input voltages of negative 36V to negative 75V, and for power levels from 30W to about 300W. The p/n for the evaluation kit is **IRDC5001-LS48V.** This evaluation kit contains detailed design considerations and in-circuit performance data for the IR5001S.

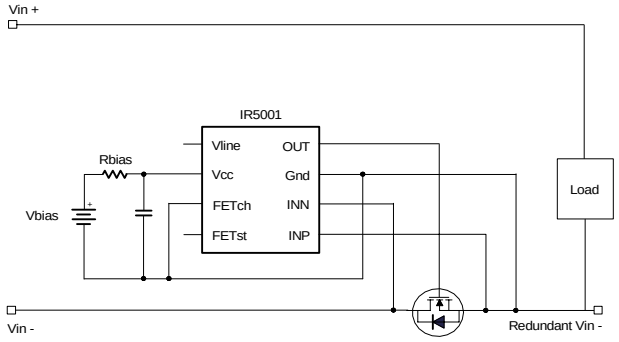


Figure. 17 Connection of INN, INP, and Gnd for negative rail Active ORing or reverse polarity protection.

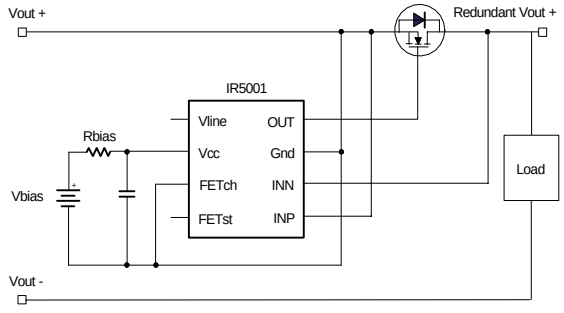


Figure. 18. Connection of INN,INP, and Gnd when the MOSFET is placed in the path of positive rail.

Positive Rail ORing / Ground ORing in Communications Boards

An example of a typical connection in positive rail ORing is shown in Fig. 18. Typical applications are inside redundant AC-DC and DC-DC power supplies, or on-board ORing. For positive rail ORing, an additional Vbias voltage above the positive rail is needed to bias the IR5001S.

An evaluation kit for high-current 12V positive rail ORing is available under p/n **IRAC5001-HS100A,** demonstrating performance of the IR5001S at 100A output current.

Considerations for the Selection of the Active ORing N-Channel MOSFET

Active ORing FET losses are all conduction losses, and depend on the source-drain current and $R_{DS(on)}$ of the FET. The conduction loss could be virtually eliminated if a FET with very low $R_{DS(on)}$ was used. However, using arbitrarily low $R_{DS(on)}$ is not desirable for three reasons:

1. Turn off propagation delay. Higher $R_{DS(on)}$ will provide more voltage information to the internal comparator, and will result in faster FET turn off protection in case of short-circuit of the source (less voltage disturbance on the redundant bus).
2. Undetected reverse (drain to source) current flow. With the asymmetrical offset voltage, some small current can flow from the drain to source of the ORing FET and be undetected by the IR5001S. The amount of undetected drain-source current depends on the $R_{DS(on)}$ of the selected MOSFET and its $R_{DS(on)}$. To keep the reverse (drain-source) current below 5 – 10% of the nominal source-drain state, the $R_{DS(on)}$ of the selected FET should produce 50mV to 100mV of the voltage drop during nominal operation.
3. Cost. With properly selected $R_{DS(on)}$, Active ORing using IR5001S can be very cost competitive with traditional ORing while providing huge power loss reduction. For example, a FET with 20mOhm $R_{DS(on)}$ results in 60mV voltage drop at 3A; associated power savings compared to the traditional diode ORing (assuming typical 0.6V forward voltage drop) is ten fold(0.18W vs. 1.8W)! Now assume that FET $R_{DS(on)}$ was 10mOhm. The power loss would be reduced by additional 90mW, which is negligible compared to the power loss reduction already achieved with 20mOhm FET. But to get this negligible saving, the cost of the Active ORing FET would increase significantly.

In a well - designed Active ORing circuit, the Rds(on) of the Active ORing FET should generate between 50mV to 100mV of (INP – INN) voltage during normal, steady state operation. (The normal operation refers to current flowing from the source to drain of the Active ORing FET, half of the full-load system current flowing through each OR-ed source, at nominal input voltage). Maximum power dissipation under worst-case conditions for the FET should be calculated and verified against the data sheet limits of the selected device.

IR5001S Thermal considerations

Maximum junction temperature of the IR5001S in an application should not exceed the maximum operating junction temperature, specified at 125°C:

Tj = Pdiss * Rtheta j-a + Tamb <= Tj (max),

where Rtheta j-a is the thermal resistance from junction to ambient thermal resistance (specified at 128 °C/W), Pdiss is IC power dissipation, and Tamb is operating ambient temperature.

The maximum power dissipation can be estimated as follows:

Pdiss < (Tj max – Tamb max) / Rtheta j-a

Since Tj max= 125 °C, Tamb = 85 °C, and Rtheta j-a = 128 °C/W, the maximum power dissipation allowed is:

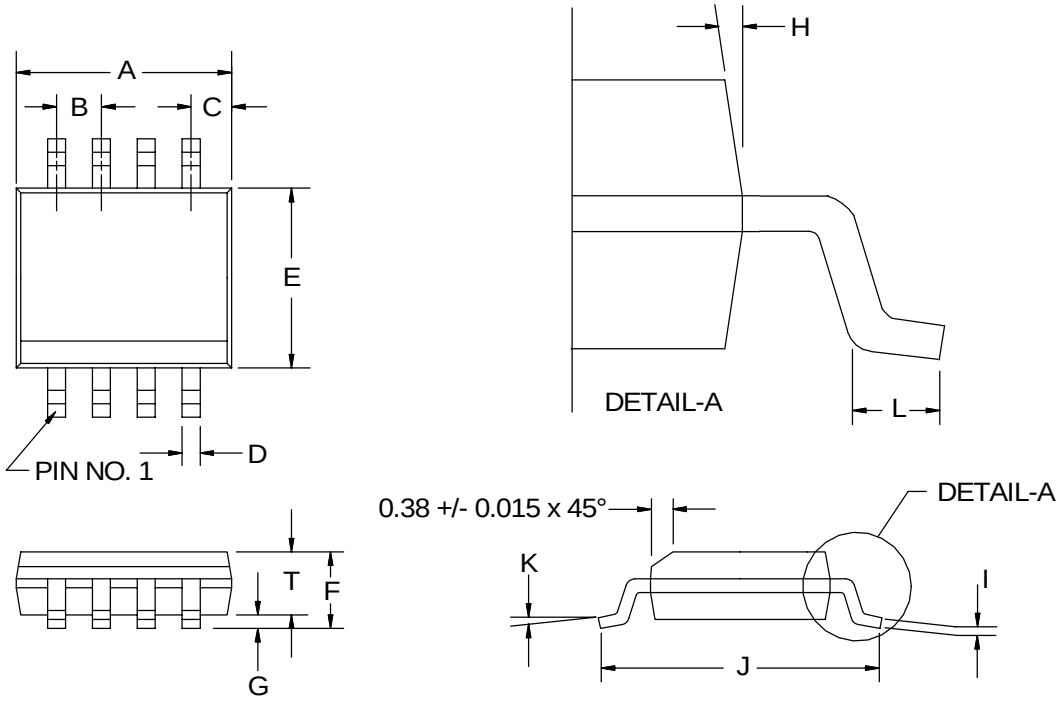
Pdiss max = (125 – 85) / 128 = 0.3W

With proper selection of Icc (as discussed in the Detailed Pin Description), the maximum power dissipation will never be exceeded (Max Icc * Max Vcc = 10mA * 13.9V = 0.14W).

Layout Considerations

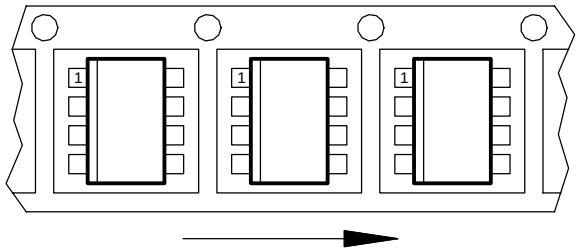
INN and INP should be connected very close to the drain and source terminal of the Active ORing FET. PCB trace between the Vout pin and the gate of the N-FET should also be minimized. A minimum of 0.1uF decoupling capacitor must be connected from Vcc to Gnd of the IR5001S and should be placed as close to the IR5001S as possible. Ground should be connected to the source of N-FET separately from the INP pin.

(S) SOIC Package
8-Pin Surface Mount, Narrow Body



8-PIN		
SYMBOL	MIN	MAX
A	4.80	4.98
B	1.27 BSC	
C	0.53 REF	
D	0.36	0.46
E	3.81	3.99
F	1.52	1.72
G	0.10	0.25
H	7° BSC	
I	0.19	0.25
J	5.80	6.20
K	0°	8°
L	0.41	1.27
T	1.37	1.57

NOTE: ALL MEASUREMENTS ARE IN MILLIMETERS.



Feed Direction
Figure A

International
IOR Rectifier

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