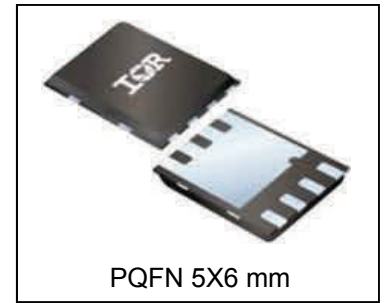
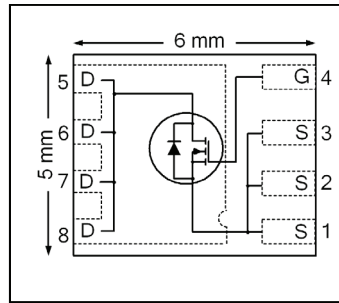


HEXFET® Power MOSFET

V_{DSS}	100	V
R_{DS(on)} max (@ V _{GS} = 10V)	4.8	mΩ
Q_g (typical)	36	nC
R_g (typical)	1.2	Ω
I_D (@T _{C(Bottom)} = 25°C)	128	A



PQFN 5X6 mm

Applications

- Optimized for Secondary Side Synchronous Rectification
- Primary Switch for High Frequency 48V/60V Telecom DC-DC Power Supplies
- Hot Swap and Active O-Ring
- BLDC Motor Drive

Features

Low R _{DS(ON)} (< 4.8mΩ)
Internal Snubber
Low Thermal Resistance to PCB (<0.8°C/W)
100% R _g Tested
Low Profile (<1.05 mm)
Industry-Standard Pinout
Compatible with Existing Surface Mount Techniques
RoHS Compliant, Halogen-Free
MSL1

results in
⇒

Benefits

Lower Conduction Losses
Reduced V _{ds} Spike, Improved EMI
Increased Power Density
Increased Reliability
Increased Power Density
Multi-Vendor Compatibility
Easier Manufacturing
Environmentally Friendlier
Increased Reliability

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFH7184PbF	PQFN 5mm x 6 mm	Tape and Reel	4000	IRFH7184TRPbF

Absolute Maximum Ratings

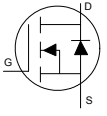
	Parameter	Max.	Units
V _{GS}	Gate-to-Source Voltage	± 20	V
I _D @ T _A = 25°C	Continuous Drain Current, V _{GS} @ 10V	20	A
I _D @ T _{C(Bottom)} = 25°C	Continuous Drain Current, V _{GS} @ 10V	128	
I _D @ T _{C(Bottom)} = 100°C	Continuous Drain Current, V _{GS} @ 10V	81	
I _{DM}	Pulsed Drain Current ①	260	
P _D @ T _A = 25°C	Power Dissipation	3.9	W
P _D @ T _{C(Bottom)} = 25°C	Power Dissipation	156	
	Linear Derating Factor	0.03	W/°C
T _J T _{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C

Notes ① through ⑤ are on page 8

Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	54	—	mV/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	4.0	4.8	m Ω	$V_{GS} = 10V, I_D = 50A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	3.6	V	$V_{DS} = V_{GS}, I_D = 150\mu A$
$\Delta V_{GS(th)}$	Gate Threshold Voltage Coefficient	—	-5.4	—	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 80V, V_{GS} = 0V$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
g_{fs}	Forward Transconductance	117	—	—	S	$V_{DS} = 25V, I_D = 50A$
Q_g	Total Gate Charge	—	36	54	nC	$V_{DS} = 50V$ $V_{GS} = 10V$ $I_D = 50A$
Q_{gs1}	Pre-V _{th} Gate-to-Source Charge	—	7.3	—		
Q_{gs2}	Post-V _{th} Gate-to-Source Charge	—	2.7	—		
Q_{gd}	Gate-to-Drain Charge	—	11	—		
Q_{godr}	Gate Charge Overdrive	—	15	—		
Q_{sw}	Switch Charge ($Q_{gs2} + Q_{gd}$)	—	13.7	—		
Q_{oss}	Output Charge	—	120	—	nC	$V_{DS} = 50V, V_{GS} = 0V$
R_G	Gate Resistance	—	1.2	2.2	Ω	
$t_{d(on)}$	Turn-On Delay Time	—	6.5	—	ns	$V_{DD} = 50V, V_{GS} = 10V$ $I_D = 50A$ $R_G = 1.0\Omega$
t_r	Rise Time	—	9.9	—		
$t_{d(off)}$	Turn-Off Delay Time	—	14	—		
t_f	Fall Time	—	3.9	—		
C_{iss}	Input Capacitance	—	2320	—	pF	$V_{GS} = 0V$ $V_{DS} = 50V$ $f = 1.0\text{MHz}$
C_{oss}	Output Capacitance	—	1070	—		
C_{rss}	Reverse Transfer Capacitance	—	19	—		

Diode Characteristics

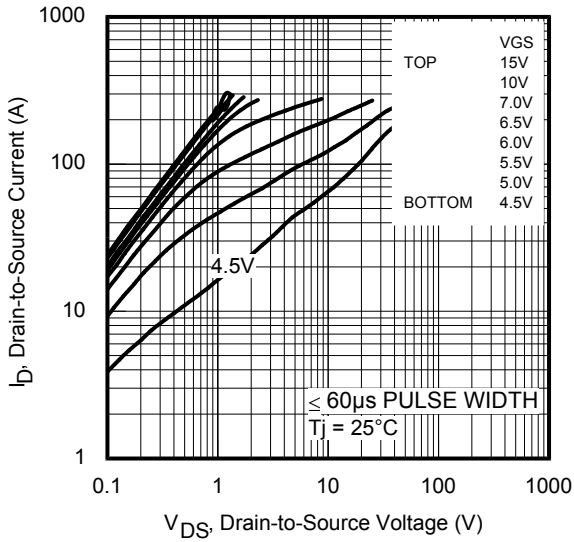
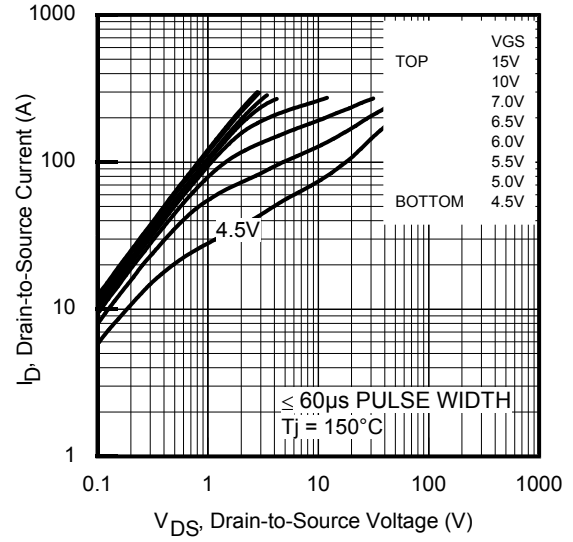
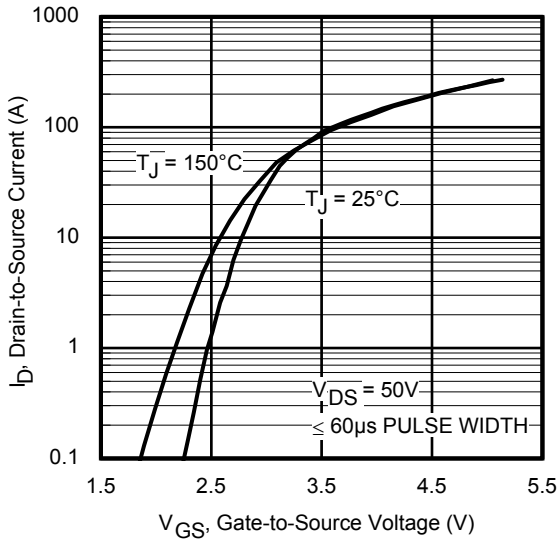
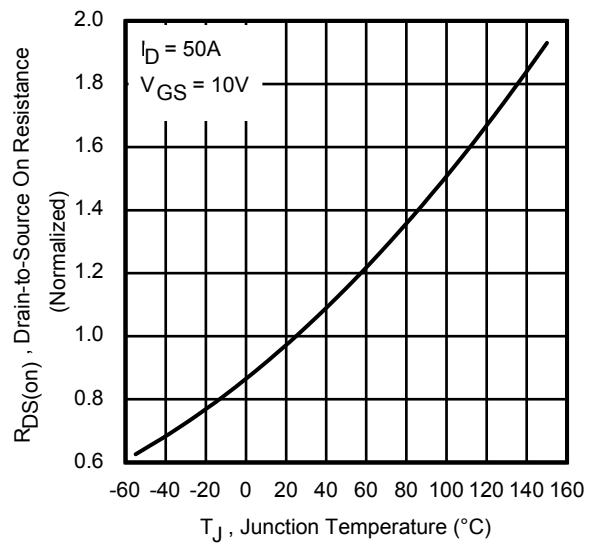
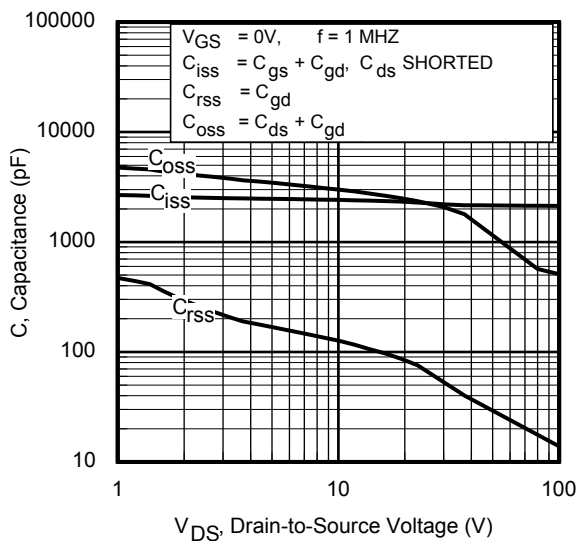
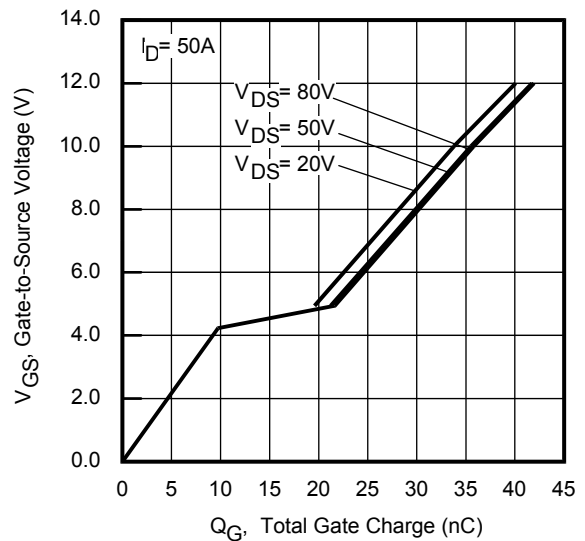
	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	128	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	260		
V_{SD}	Diode Forward Voltage	—	0.8	1.3	V	$T_J = 25^\circ\text{C}, I_S = 50A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	—	55	83	ns	$T_J = 25^\circ\text{C}, I_F = 50A, V_{DD} = 50V$
Q_{rr}	Reverse Recovery Charge	—	76	114	nC	$di/dt = 100A/\mu s$ ③

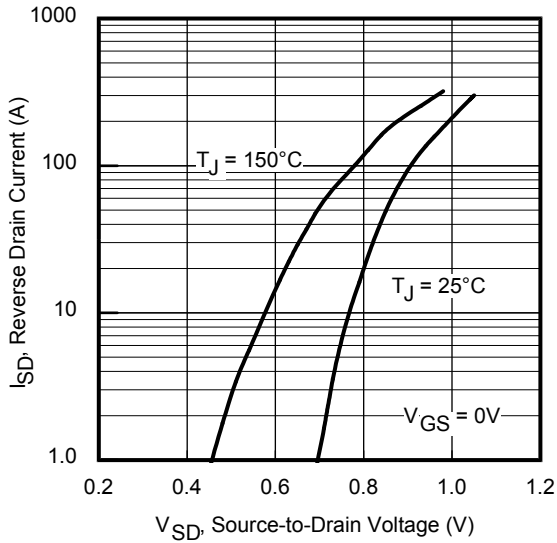
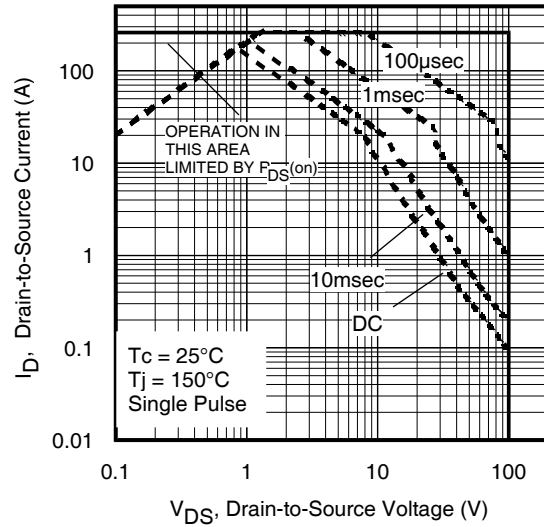
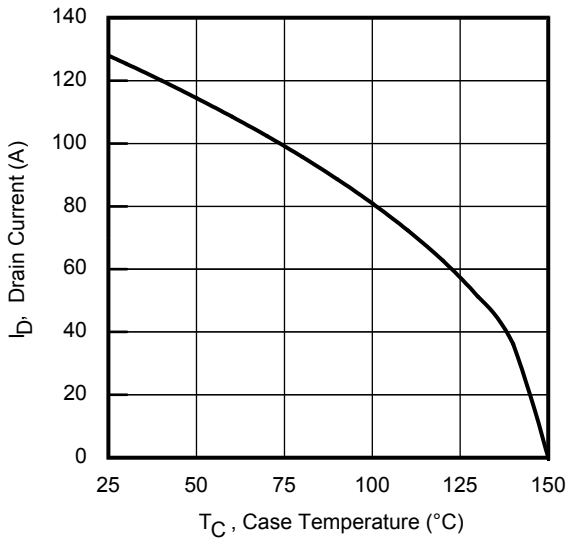
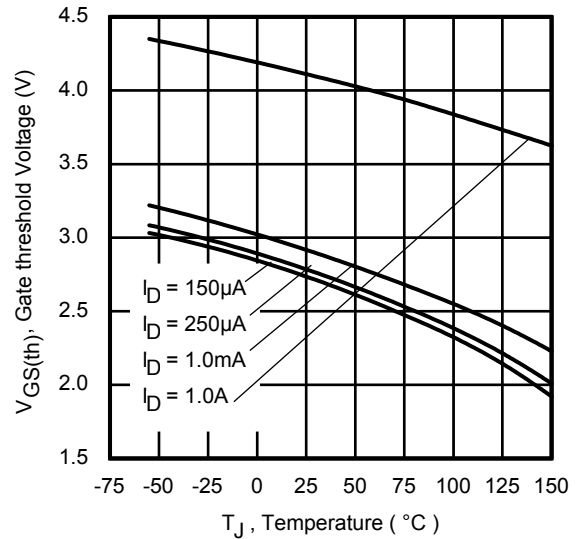
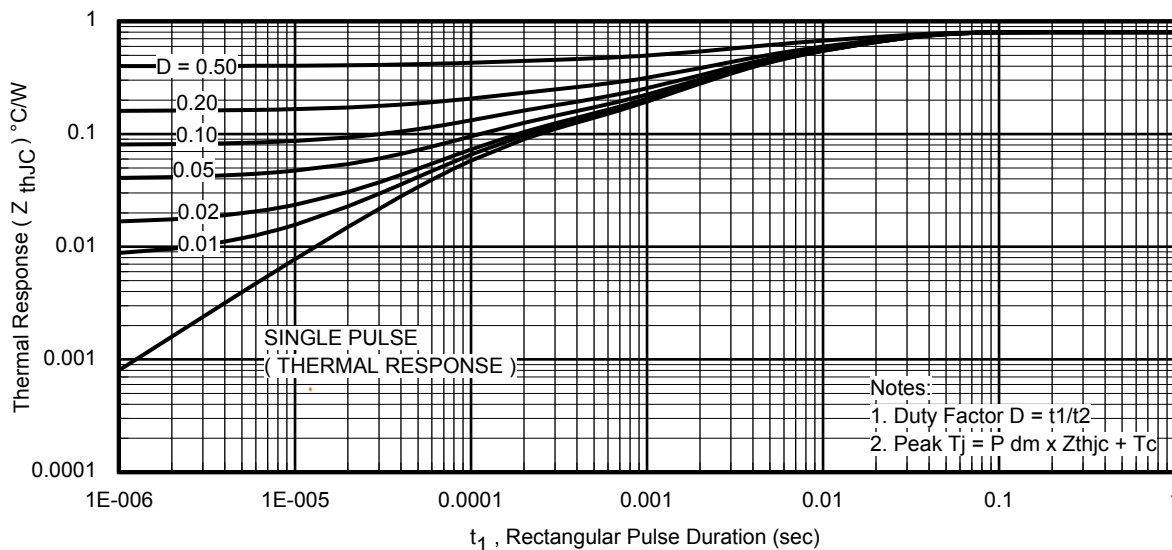
Avalanche Characteristics

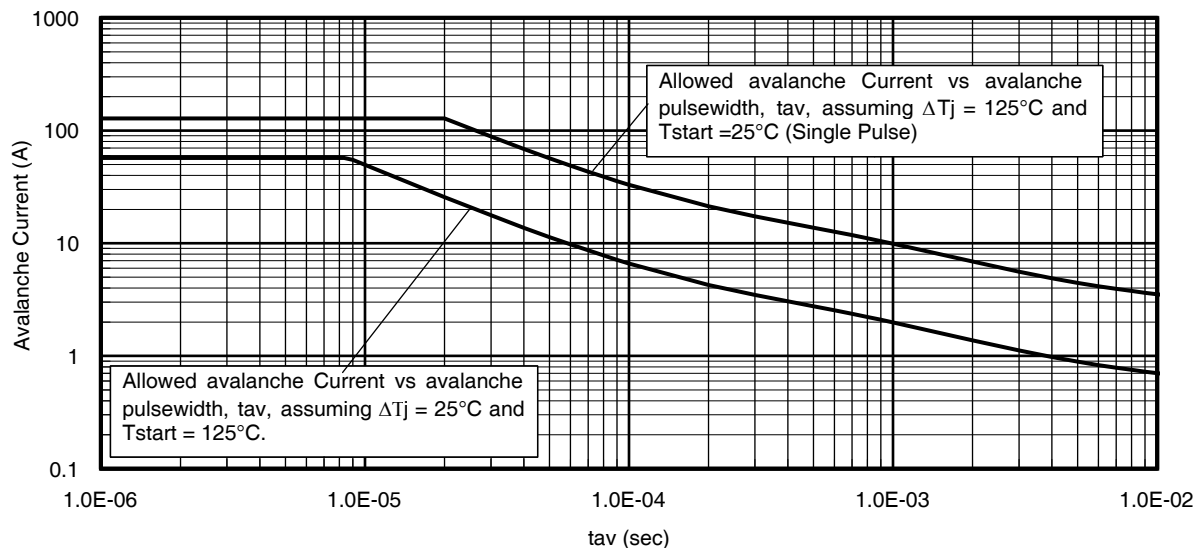
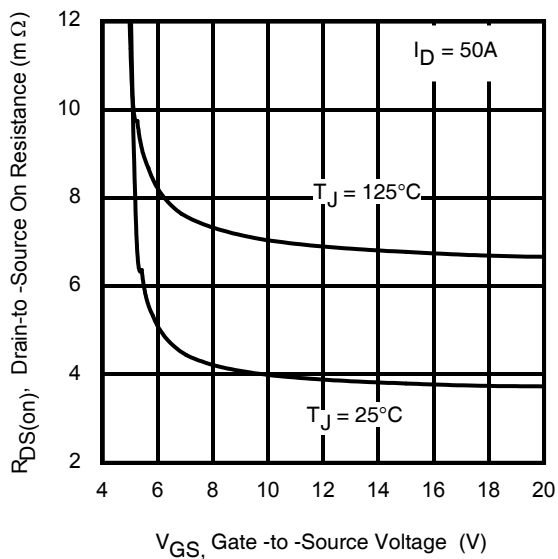
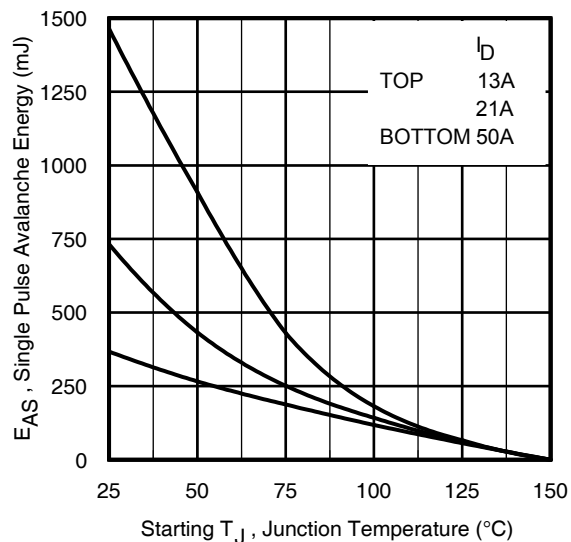
	Parameter	Typ.	Max.	Units
E_{AS} (Thermally limited)	Single Pulse Avalanche Energy ②	—	360	mJ
I_{AR}	Avalanche Current ①	—	50	A

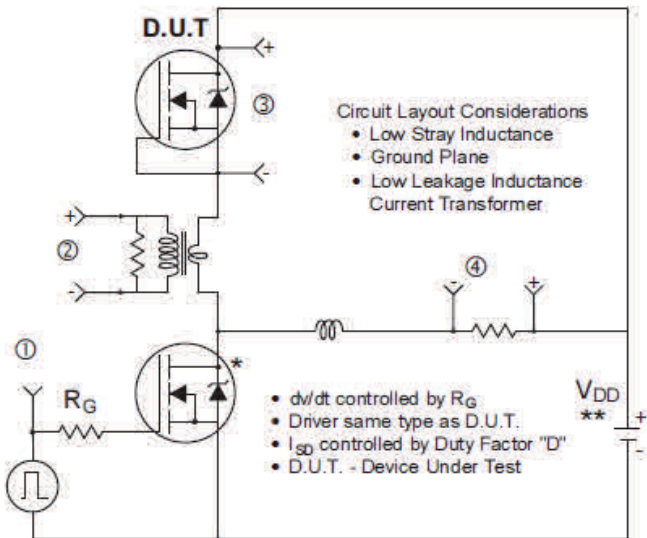
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case ④	—	0.8	°C/W
$R_{\theta JC}$ (Top)	Junction-to-Case ④	—	21	
$R_{\theta JA}$	Junction-to-Ambient ⑤	—	32	
$R_{\theta JA} (<10s)$	Junction-to-Ambient ⑤	—	19	


Fig 1. Typical Output Characteristics

Fig 2. Typical Output Characteristics

Fig 3. Typical Transfer Characteristics

Fig 4. Normalized On-Resistance vs. Temperature

Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage


Fig 7. Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area

Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10. Threshold Voltage vs. Temperature

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig 12. Typical Avalanche Current vs. Pulse Width

Fig 13. On-Resistance vs. Gate Voltage

Fig 14. Maximum Avalanche Energy vs. Drain Current

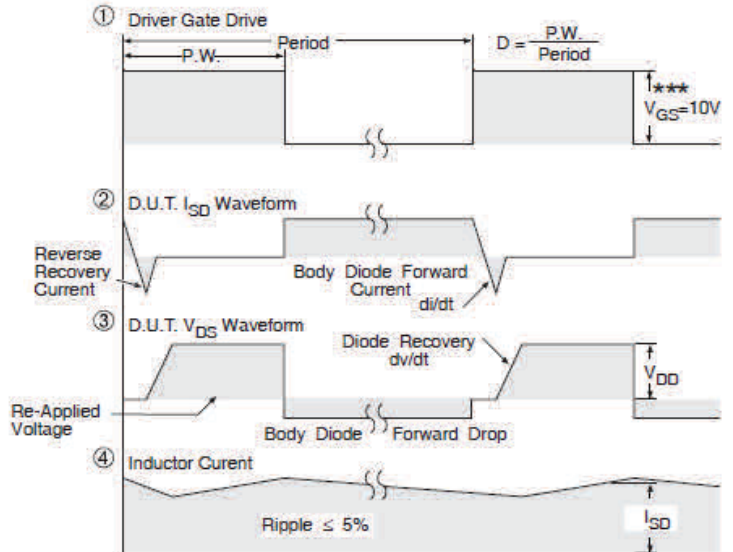


- Circuit Layout Considerations**
- Low Stray Inductance
 - Ground Plane
 - Low Leakage Inductance
 - Current Transformer

- dv/dt controlled by R_G
- Driver same type as D.U.T.
- I_{SD} controlled by Duty Factor "D"
- D.U.T. - Device Under Test

* Use P-Channel Driver for P-Channel Measurements

** Reverse Polarity for P-Channel



*** $V_{GS} = 5V$ for Logic Level Devices

Fig 15. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

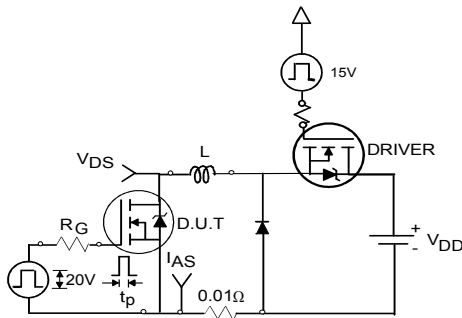


Fig 16a. Unclamped Inductive Test Circuit

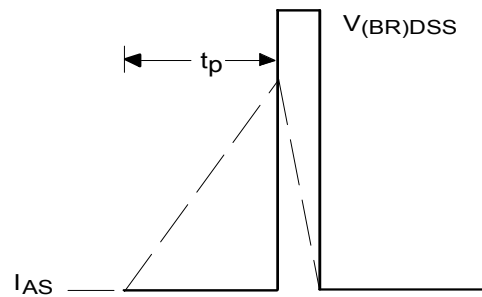


Fig 16b. Unclamped Inductive Waveforms

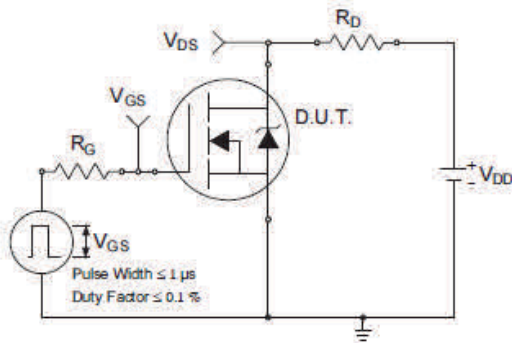


Fig 17a. Switching Time Test Circuit

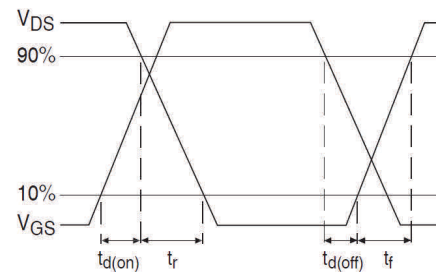


Fig 17b. Switching Time Waveforms

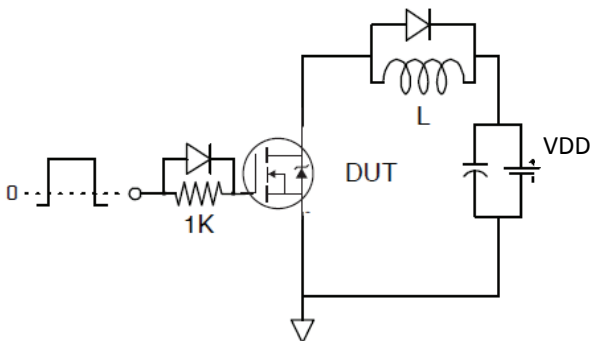


Fig 18. Gate Charge Test Circuit

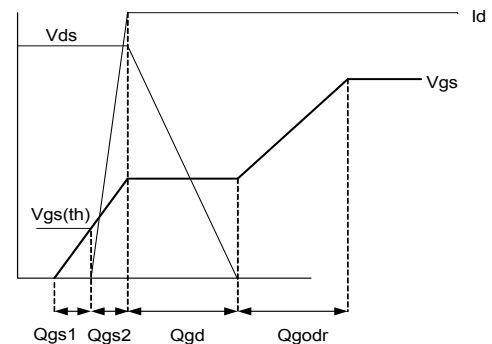
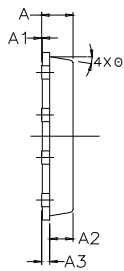
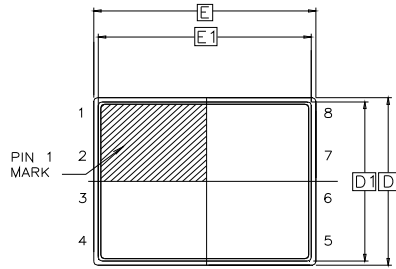


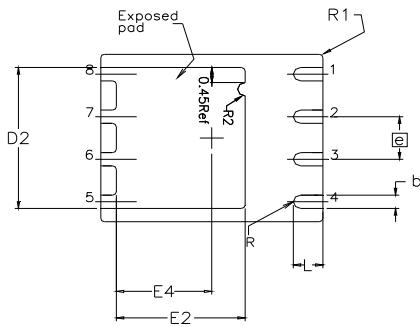
Fig 19. Gate Charge Waveform

PQFN 5x6 Outline "B" Package Details


SIDE VIEW



TOP VIEW



BOTTOM VIEW

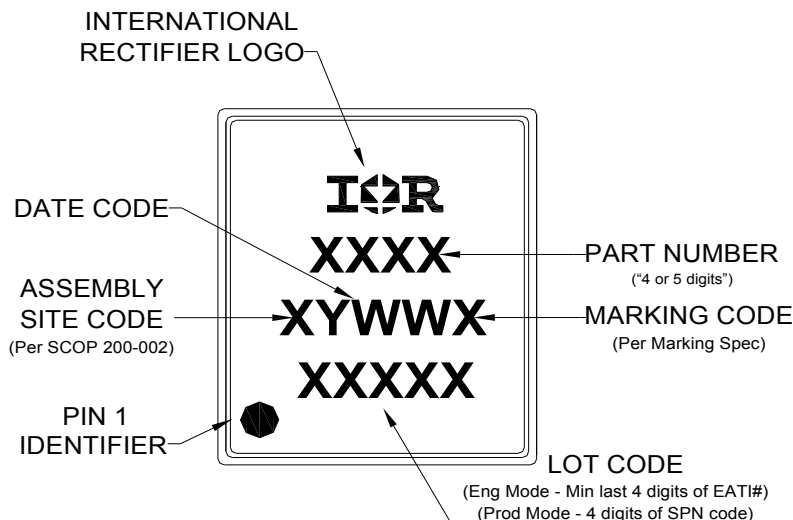
DIM SYMBOL	MILLIMETERS		INCH	
	MIN	MAX	MIN	MAX
A	0.800	1.050	0.0315	0.0413
A1	0.000	0.050	0.0000	0.0020
A2	0.580	0.680	0.0228	0.0268
A3	0.254	REF	0.0100	REF
A4	0.127	REF	0.0050	REF
D	4.850	5.150	0.1909	0.2028
D1	4.675	5.000	0.1841	0.1969
D2	3.700	4.300	0.1457	0.1693
E	5.850	6.150	0.2303	0.2421
E1	5.675	6.000	0.2234	0.2362
E2	3.380	3.780	0.1331	0.1488
E4	2.480	2.680	0.0976	0.2362
R	0.200	REF	0.0079	REF
R1	0.100	REF	0.0039	REF
R2	0.150	0.200	0.0059	0.0079
L	0.510	0.900	0.0201	0.0354
b	0.310	0.510	0.0122	0.0201
b1	0.025	0.125	0.0010	0.0049
b2	0.210	0.410	0.0083	0.0161
b3	0.150	0.450	0.0059	0.0177
e	1.270	REF	0.0500	REF
e1	2.800	REF	0.1102	REF
P	0°	12°	0°	12°
K	1.200	1.420	0.0472	0.0559

Note:

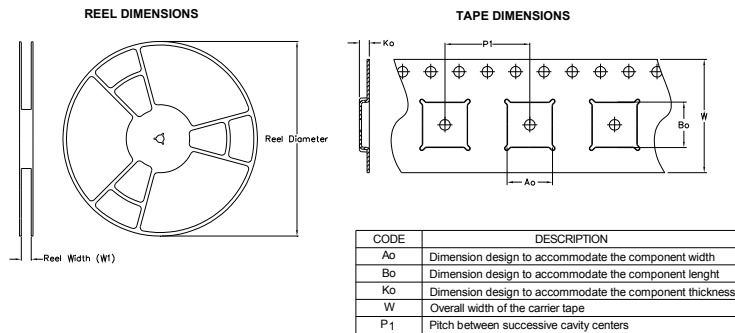
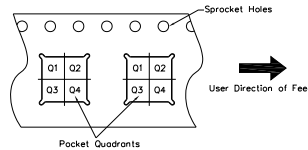
1. Dimensions and tolerancing confirm to ASME Y14.5M-1994
2. Dimension L represents terminal full back from package edge up to 0.1mm is acceptable
3. Coplanarity applies to the expose Heat Slug as well as the terminal
4. Radius on terminal is Optional

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: <http://www.irf.com/technical-info/appnotes/an-1136.pdf>

For more information on package inspection techniques, please refer to application note AN-1154: <http://www.irf.com/technical-info/appnotes/an-1154.pdf>

PQFN 5x6 Outline "B" Part Marking


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

PQFN 5x6 Outline "B" Tape and Reel

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


Note: All dimension are nominal

Package Type	Reel Diameter (Inch)	QTY	Reel Width W1 (mm)	Ao (mm)	Bo (mm)	Ko (mm)	P1 (mm)	W (mm)	Pin 1 Quadrant
5 X 6 PQFN	13	4000	12.4	6.300	5.300	1.20	8.00	12	Q1

 Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>
Qualification Information[†]

Qualification Level	Industrial (per JEDEC JESD47F ^{††} guidelines)	
Moisture Sensitivity Level	PQFN 5mm x 6mm	MSL1 (per JEDEC J-STD-020D ^{††})
RoHS Compliant	Yes	

[†] Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>
^{††} Applicable version of JEDEC standard at the time of product release.

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 290\mu\text{H}$, $R_G = 50\Omega$, $I_{AS} = 50\text{A}$.
- ③ Pulse width $\leq 400\mu\text{s}$; duty cycle $\leq 2\%$.
- ④ R_θ is measured at T_J of approximately 90°C .
- ⑤ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details: <http://www.irf.com/technical-info/appnotes/an-994.pdf>

Revision History

Date	Comments
01/06/2015	• Flg 8 SOA Curve is corrected — The label PW = 1msec and 10msec are switched—page 4.

Mouser Electronics

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[IRFH7184TRPBF](#)