



MICROCHIP PIC18F2XJXX/4XJXX FAMILY

Flash Microcontroller Programming Specification

1.0 DEVICE OVERVIEW

This document includes the programming specifications for the following devices:

- PIC18F24J10
- PIC18F25J10
- PIC18F44J10
- PIC18F45J10
- PIC18F24J11
- PIC18F25J11
- PIC18F26J11
- PIC18F44J11
- PIC18F45J11
- PIC18F46J11
- PIC18F26J13
- PIC18F27J13
- PIC18F46J13
- PIC18F47J13
- PIC18F24J50
- PIC18F25J50
- PIC18F26J50
- PIC18F44J50
- PIC18F45J50
- PIC18F46J50
- PIC18F26J53
- PIC18F27J53
- PIC18F46J53
- PIC18F47J53
- PIC18LF24J10
- PIC18LF25J10
- PIC18LF44J10
- PIC18LF45J10
- PIC18LF24J11
- PIC18LF25J11
- PIC18LF26J11
- PIC18LF44J11
- PIC18LF45J11
- PIC18LF46J11
- PIC18LF26J13
- PIC18LF27J13
- PIC18LF46J13
- PIC18LF47J13
- PIC18LF24J50
- PIC18LF25J50
- PIC18LF26J50
- PIC18LF44J50
- PIC18LF45J50
- PIC18LF46J50
- PIC18LF26J53
- PIC18LF27J53
- PIC18LF46J53
- PIC18LF47J53

2.0 PROGRAMMING OVERVIEW OF THE PIC18F2XJXX/4XJXX FAMILY

The PIC18F2XJXX/4XJXX family devices are programmed using In-Circuit Serial Programming™ (ICSP™). This programming specification applies to devices of the PIC18F2XJXX/4XJXX family in all package types.

2.1 Pin Diagrams

The pin diagrams for the PIC18F2XJXX/4XJXX family are shown in Figure 2-1 and Figure 2-2. The pins that are required for programming are listed in Table 2-1 and shown in darker lettering in the diagrams.

TABLE 2-1: PIN DESCRIPTIONS (DURING PROGRAMMING): PIC18F2XJXX/4XJXX FAMILY

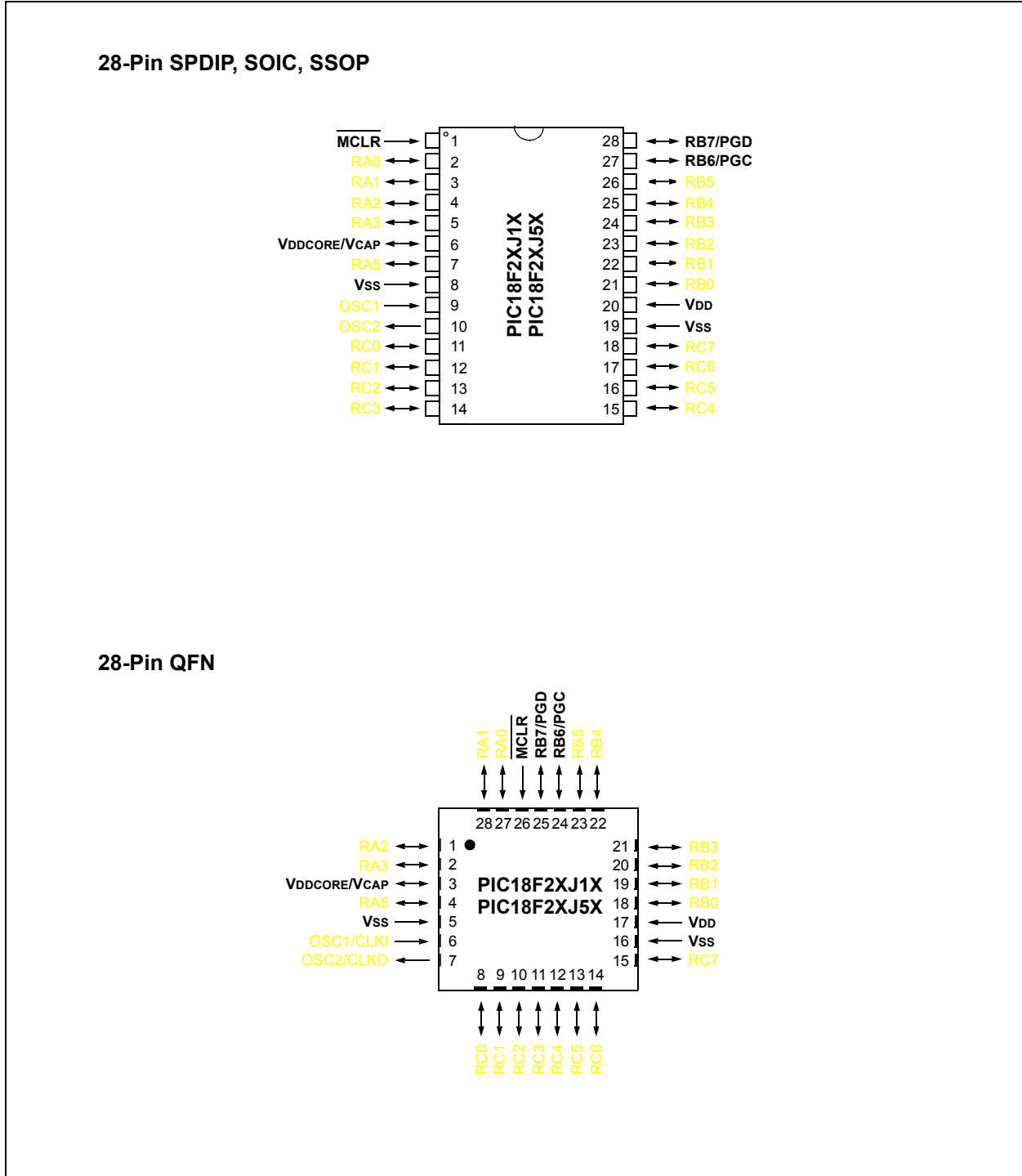
| Pin Name | During Programming | | |
|-----------------------------|--------------------|----------|---|
| | Pin Name | Pin Type | Pin Description |
| MCLR | MCLR | P | Programming Enable |
| VDD and AVDD ⁽¹⁾ | VDD | P | Power Supply |
| VSS and AVSS ⁽¹⁾ | VSS | P | Ground |
| VDDCORE/VCAP | VDDCORE | P | Regulated Power Supply for Microcontroller Core |
| | VCAP | I | Filter Capacitor for On-Chip Voltage Regulator |
| RB6 | PGC | I | Serial Clock |
| RB7 | PGD | I/O | Serial Data |

Legend: I = Input, O = Output, P = Power

Note 1: All power supply and ground pins must be connected, including analog supplies (AVDD) and ground (AVSS).

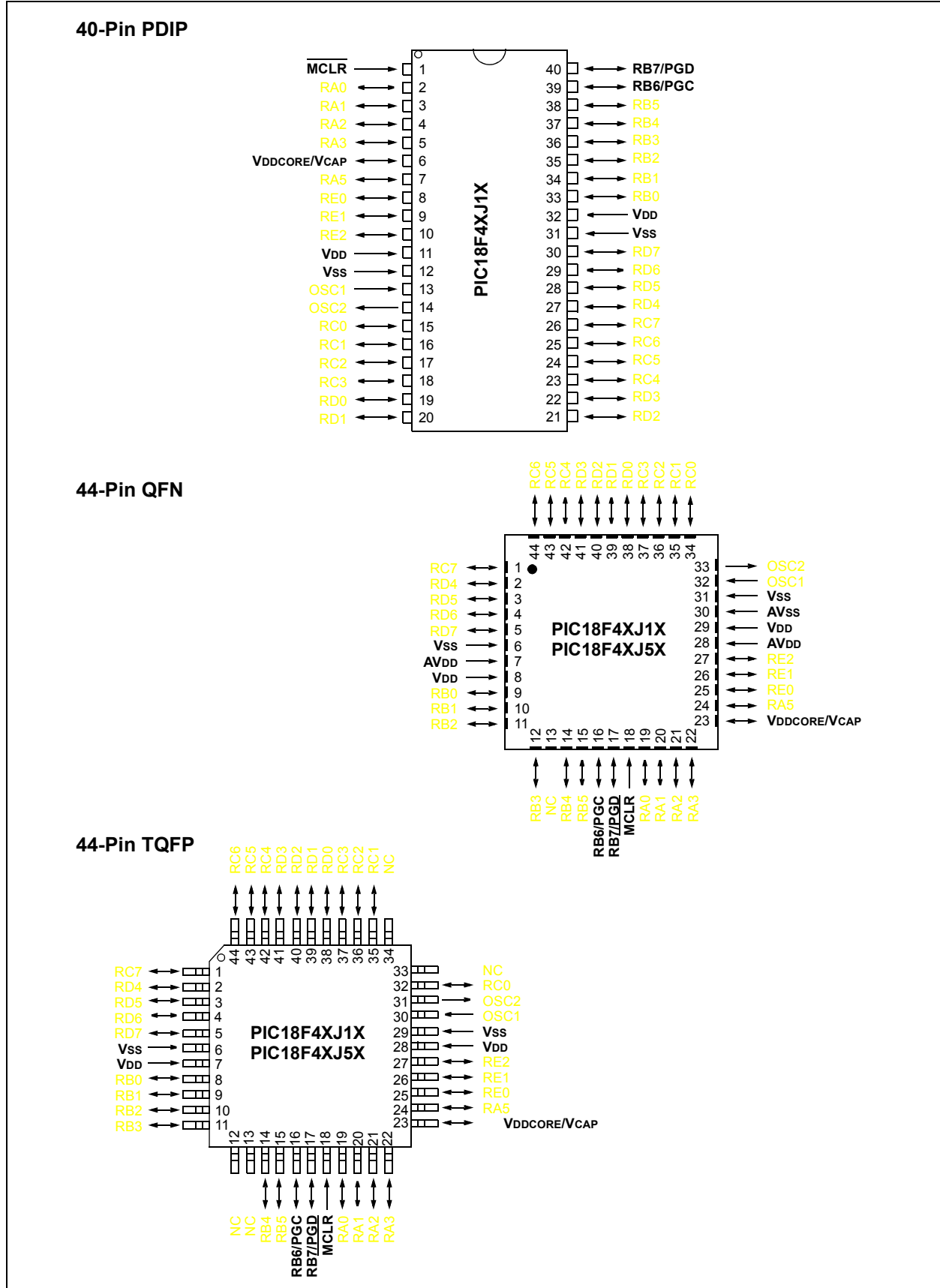
PIC18F2XJXX/4XJXX FAMILY

FIGURE 2-1: PIC18F2XJXX/4XJXX FAMILY PIN DIAGRAMS



PIC18F2XJXX/4XJXX FAMILY

FIGURE 2-2: PIC18F2XJXX/4XJXX FAMILY PIN DIAGRAMS (CONTINUED)



PIC18F2XJXX/4XJXX FAMILY

2.1.1 PIC18F2XJXX/4XJXX/ LF2XJXX/LF4XJXX DEVICES AND THE ON-CHIP VOLTAGE REGULATOR

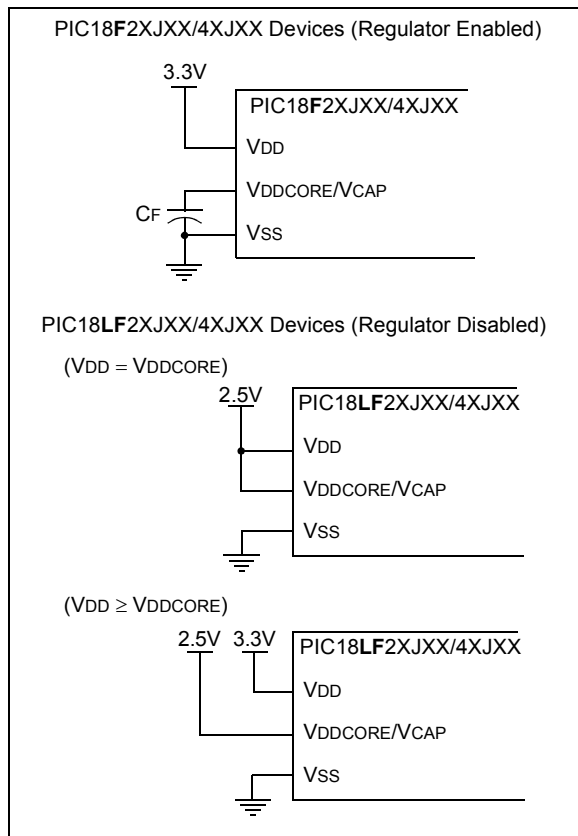
PIC18FXXJXX devices have an internal core voltage regulator. On these devices (“PIC18F” in the part number), the regulator is always enabled. The regulator input is taken from the microcontroller VDD pins. The output of the regulator is supplied to the VDDCORE/VCAP pin. On these devices, this pin simultaneously serves as both the regulator output and the microcontroller core power input pin. For these devices, the VDDCORE/VCAP pin should be tied to a capacitor and nothing else.

PIC18LFXJXX devices do not have an internal core voltage regulator. On these devices (“PIC18LF” in the part number), power must be externally supplied to both VDD and VDDCORE/VCAP.

Whether or not the regulator is used, it is always good design practice to have sufficient capacitance on all supply pins. Examples are shown in Figure 2-3.

The specifications for core voltage and capacitance are listed in **Section 6.0 “AC/DC Characteristics Timing Requirements for Program/Verify Test Mode”**.

FIGURE 2-3: CONNECTIONS FOR THE ON-CHIP REGULATOR



2.2 Memory Maps

The PIC18F2XJXX/4XJXX family of devices offers program memory sizes of 16, 32, 64 and 128 Kbytes. The memory sizes for different members of the family are shown in Table 2-2. The overall memory maps for all the devices are shown in Figure 2-4.

TABLE 2-2: PROGRAM MEMORY SIZES FOR PIC18F2XJXX/4XJXX FAMILY DEVICES

| Device* | Program Memory (Kbytes) | Location of Flash Configuration Words |
|-------------|-------------------------|---------------------------------------|
| PIC18F24J10 | 16 | 3FF8h:3FFFh |
| PIC18F44J10 | | |
| PIC18F24J11 | | |
| PIC18F44J11 | | |
| PIC18F24J50 | | |
| PIC18F44J50 | | |
| PIC18F25J10 | 32 | 7FF8h:7FFFh |
| PIC18F45J10 | | |
| PIC18F25J11 | | |
| PIC18F45J11 | | |
| PIC18F25J50 | | |
| PIC18F45J50 | | |
| PIC18F26J11 | 64 | FFF8h:FFFFh |
| PIC18F46J11 | | |
| PIC18F26J13 | | |
| PIC18F46J13 | | |
| PIC18F26J50 | | |
| PIC18F46J50 | | |
| PIC18F26J53 | 128 | 1FFF8h:1FFFFh |
| PIC18F46J53 | | |
| PIC18F27J13 | | |
| PIC18F47J13 | | |
| PIC18F27J53 | | |
| PIC18F47J53 | | |

* Includes PIC18F and PIC18LF devices.

For purposes of code protection, the program memory for every device is treated as a single block. Enabling code protection, thus protects the entire code memory, and not individual segments.

PIC18F2XJXX/4XJXX FAMILY

The Configuration Words for these devices are located at addresses, 300000h through 300007h. These are implemented as three pairs of volatile memory registers. Each register is automatically loaded from a copy stored at the end of program memory. For this reason, the last four words (or eight bytes) of the code space (also called the Flash Configuration Words) should be written with configuration data and not executable code. The addresses of the Flash Configuration Words are also listed in Table 2-2. Refer to section **Section 5.0 “Configuration Word”** for more information.

Locations, 3FFFEh and 3FFFFh, are reserved for the device ID bits. These bits may be used by the programmer to identify what device type is being programmed and are described in **Section 5.1 “Device ID Word”**. These device ID bits read out normally, even after code protection.

2.2.1 MEMORY ADDRESS POINTER

Memory in the device address space (000000h to 3FFFFFFh) is addressed via the Table Pointer register, which in turn, is comprised of three registers:

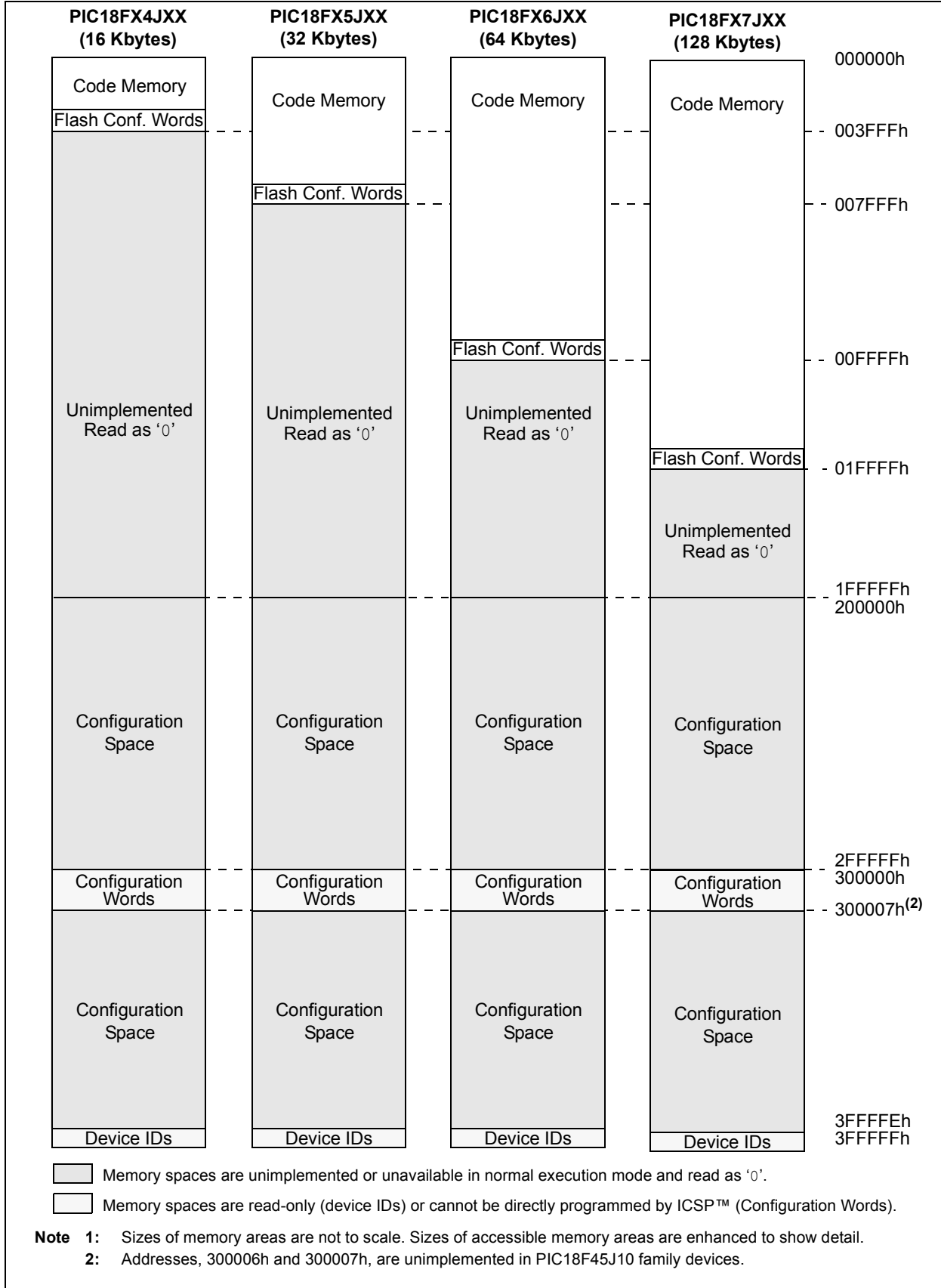
- TBLPTRU at RAM address 0FF8h
- TBLPTRH at RAM address 0FF7h
- TBLPTRL at RAM address 0FF6h

| TBLPTRU | TBLPTRH | TBLPTRL |
|-------------|------------|-----------|
| Addr[21:16] | Addr[15:8] | Addr[7:0] |

The 4-bit command, '0000' (core instruction), is used to load the Table Pointer prior to using many read or write operations.

PIC18F2XJXX/4XJXX FAMILY

FIGURE 2-4: MEMORY MAPS FOR PIC18F2XJXX/4XJXX FAMILY DEVICES⁽¹⁾

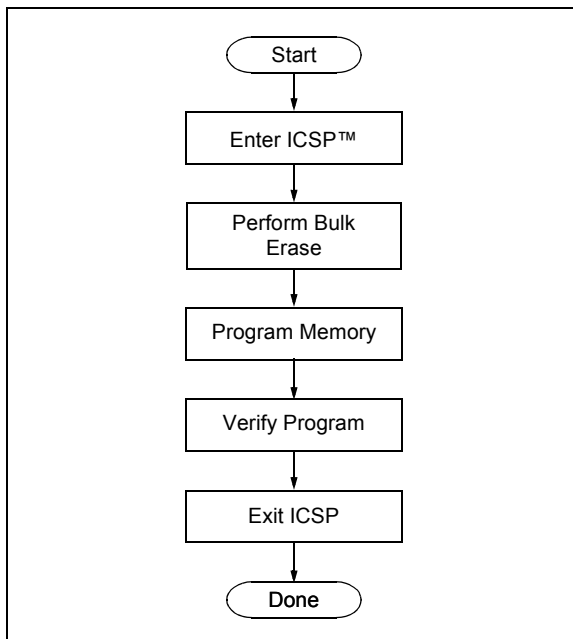


PIC18F2XJXX/4XJXX FAMILY

2.3 Overview of the Programming Process

Figure 2-5 shows the high-level overview of the programming process. First, a Bulk Erase is performed. Next, the code memory is programmed. Since the only nonvolatile Configuration Words are within the code memory space, they too are programmed as if they were code. Code memory (including the Configuration Words) is then verified to ensure that programming was successful.

FIGURE 2-5: HIGH-LEVEL PROGRAMMING FLOW



2.4 Entering and Exiting ICSP™ Program/Verify Mode

Entry into ICSP modes for PIC18F2XJXX/4XJXX family devices is somewhat different than previous PIC18 devices. As shown in Figure 2-6, entering ICSP Program/Verify mode requires three steps:

1. Voltage is briefly applied to the $\overline{\text{MCLR}}$ pin.
2. A 32-bit key sequence is presented on PGD.
3. Voltage is reapplied to $\overline{\text{MCLR}}$ and held.

The programming voltage applied to $\overline{\text{MCLR}}$ is V_{IH} , or essentially, V_{DD} . There is no minimum time requirement for holding at V_{IH} . After V_{IH} is removed, an interval of at least P19 must elapse before presenting the key sequence on PGD.

The key sequence is a specific 32-bit pattern, '0100 1101 0100 0011 0100 1000 0101 0000' (more easily remembered as 4D434850h in hexadecimal). The device will enter Program/Verify mode only if the sequence is valid. The Most Significant bit of the most significant nibble must be shifted in first.

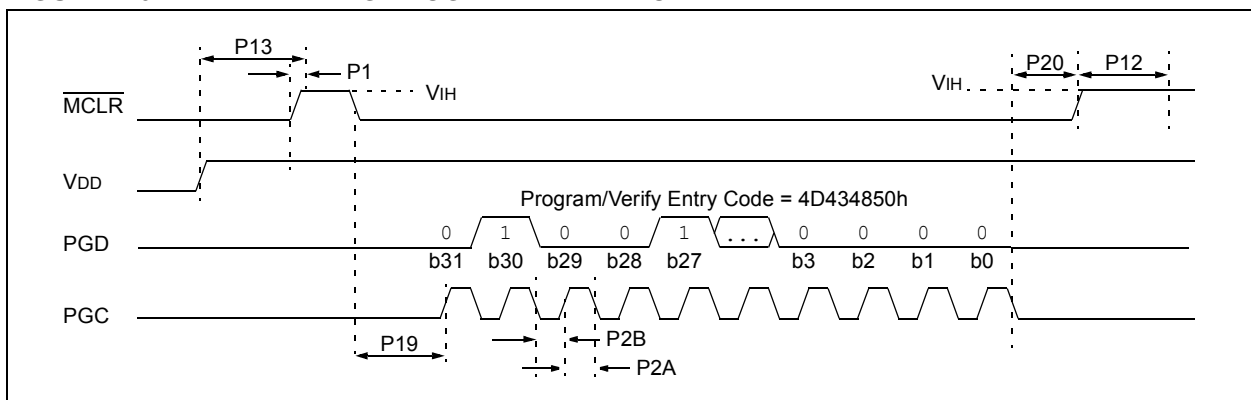
Once the key sequence is complete, V_{IH} must be applied to $\overline{\text{MCLR}}$ and held at that level for as long as Program/Verify mode is to be maintained. An interval of at least time, P20 and P12, must elapse before presenting data on PGD. Signals appearing on PGD before P12 has elapsed may not be interpreted as valid.

On successful entry, the program memory can be accessed and programmed in serial fashion. While in the Program/Verify mode, all unused I/Os are placed in the high-impedance state.

Exiting Program/Verify mode is done by removing V_{IH} from $\overline{\text{MCLR}}$, as shown in Figure 2-7. The only requirement for exit is that an interval, P16, should elapse between the last clock and program signals on PGC and PGD before removing V_{IH} .

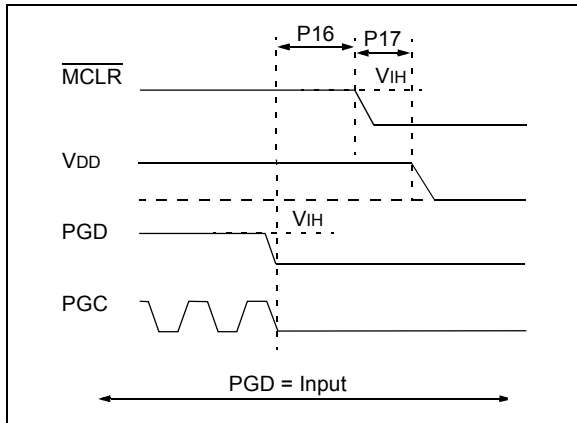
When V_{IH} is reapplied to $\overline{\text{MCLR}}$, the device will enter the ordinary operational mode and begin executing the application instructions.

FIGURE 2-6: ENTERING PROGRAM/VERIFY MODE



PIC18F2XJXX/4XJXX FAMILY

FIGURE 2-7: EXITING PROGRAM/VERIFY MODE



2.5 Serial Program/Verify Operation

The PGC pin is used as a clock input pin and the PGD pin is used for entering command bits and data input/output during serial operation. Commands and data are transmitted on the rising edge of PGC, latched on the falling edge of PGC and are Least Significant bit (LSb) first.

2.5.1 FOUR-BIT COMMANDS

All instructions are 20 bits, consisting of a leading 4-bit command followed by a 16-bit operand, which depends on the type of command being executed. To input a command, PGC is cycled four times. The commands needed for programming and verification are shown in Table 2-3.

Depending on the 4-bit command, the 16-bit operand represents 16 bits of input data or 8 bits of input data and 8 bits of output data.

Throughout this specification, commands and data are presented as illustrated in Table 2-4. The 4-bit command is shown Most Significant bit (MSb) first. The command operand, or “Data Payload”, is shown <MSB><LSB>. Figure 2-8 demonstrates how to serially present a 20-bit command/operand to the device.

2.5.2 CORE INSTRUCTION

The core instruction passes a 16-bit instruction to the CPU core for execution. This is needed to set up registers as appropriate for use with other commands.

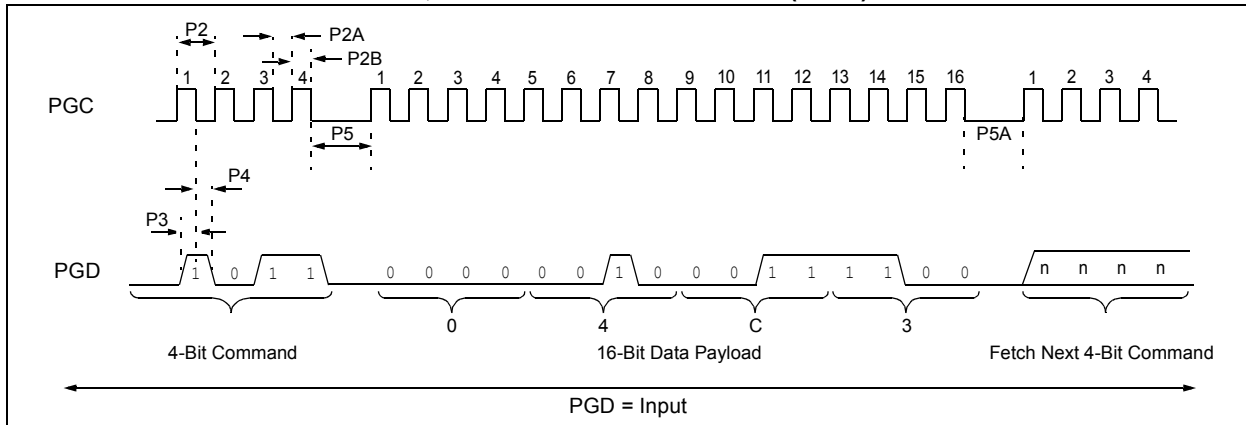
TABLE 2-3: COMMANDS FOR PROGRAMMING

| Description | 4-Bit Command |
|---|---------------|
| Core Instruction (Shift in 16-bit instruction) | 0000 |
| Shift out TABLAT register | 0010 |
| Table Read | 1000 |
| Table Read, Post-Increment | 1001 |
| Table Read, Post-Decrement | 1010 |
| Table Read, Pre-Increment | 1011 |
| Table Write | 1100 |
| Table Write, Post-Increment by 2 | 1101 |
| Table Write, Start Programming, Post-Increment by 2 | 1110 |
| Table Write, Start Programming | 1111 |

TABLE 2-4: SAMPLE COMMAND SEQUENCE

| 4-Bit Command | Data Payload | Core Instruction |
|---------------|--------------|----------------------------------|
| 1101 | 3C 40 | Table Write, post-increment by 2 |

FIGURE 2-8: TABLE WRITE, POST-INCREMENT TIMING (1101)



PIC18F2XJXX/4XJXX FAMILY

3.0 DEVICE PROGRAMMING

Programming includes the ability to erase or write the memory within the device.

The EECON1 register is used to control Write or Row Erase operations. The WREN bit must be set to enable writes; this must be done prior to initiating a write sequence. It is strongly recommended that the WREN bit only be set immediately prior to a program or erase operation.

The FREE bit must be set in order to erase the program space being pointed to by the Table Pointer. The erase or write sequence is initiated by setting the WR bit.

3.1 ICSP™ Erase

3.1.1 ICSP™ BULK ERASE

Devices of the PIC18F2XJXX/4XJXX family may be Bulk Erased by writing 0180h to the table address, 3C0005h:3C0004h. The basic sequence is shown in Table 3-1 and demonstrated in Figure 3-1.

Since the code-protect Configuration bit is stored in the program code within code memory, a Bulk Erase operation will also clear any code-protect settings for the device.

The actual Bulk Erase function is a self-timed operation. Once the erase has started (falling edge of the 4th PGC after the NOP command), serial execution will cease until the erase completes (parameter P11). During this time, PGC may continue to toggle but PGD must be held low.

TABLE 3-1: BULK ERASE COMMAND SEQUENCE

| 4-Bit Command | Data Payload | Core Instruction |
|---------------|--------------|---|
| 0000 | 0E 3C | MOVLW 3Ch |
| 0000 | 6E F8 | MOVWF TBLPTRU |
| 0000 | 0E 00 | MOVLW 00h |
| 0000 | 6E F7 | MOVWF TBLPTRH |
| 0000 | 0E 05 | MOVLW 05h |
| 0000 | 6E F6 | MOVWF TBLPTRL |
| 1100 | 01 01 | Write 01h to 3C0005h |
| 0000 | 0E 3C | MOVLW 3Ch |
| 0000 | 6E F8 | MOVWF TBLPTRU |
| 0000 | 0E 00 | MOVLW 00h |
| 0000 | 6E F7 | MOVWF TBLPTRH |
| 0000 | 0E 04 | MOVLW 04h |
| 0000 | 6E F6 | MOVWF TBLPTRL |
| 1100 | 80 80 | Write 80h to 3C0004h to erase entire device. NOP |
| 0000 | 00 00 | Hold PGD low until erase completes. |
| 0000 | 00 00 | |

FIGURE 3-1: BULK ERASE FLOW

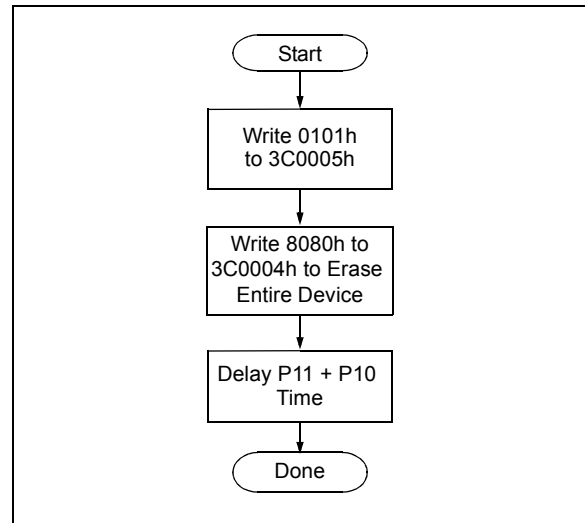
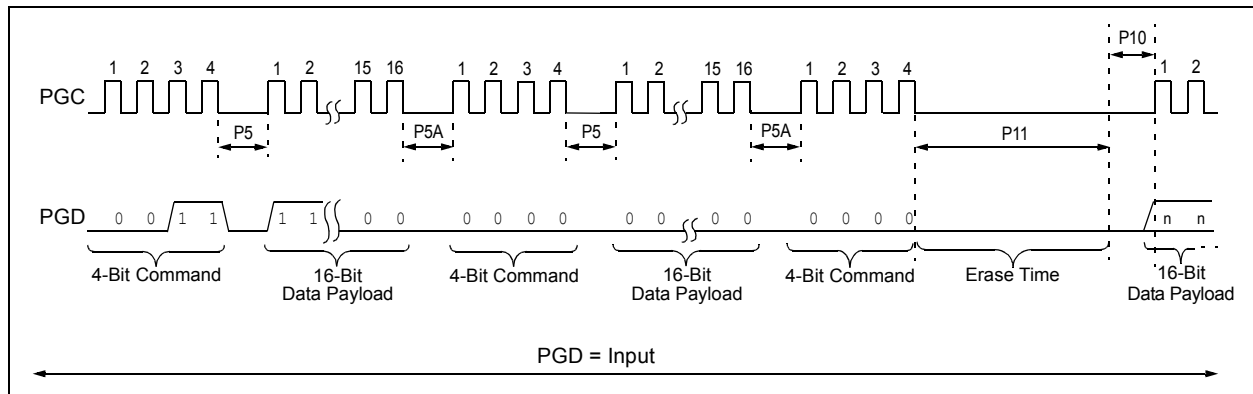


FIGURE 3-2: BULK ERASE TIMING



PIC18F2XJXX/4XJXX FAMILY

3.1.2 ICSP™ ROW ERASE

It is possible to erase one row (1024 bytes of data), provided the block is not code-protected or erase/write-protected. Rows are located at static boundaries beginning at program memory address 000000h, extending to the internal program memory limit (see Section 2.2 “Memory Maps”).

The Row Erase duration is internally timed. After the WR bit in EECON1 is set, a NOP is issued, where the 4th PGC is held high for the duration of the Row Erase time, P10.

The code sequence to Row Erase a PIC18F2XJXX/4XJXX family device is shown in Table 3-2. The flowchart shown in Figure 3-4 depicts the logic necessary to completely erase a

PIC18F2XJXX/4XJXX family device. The timing diagram that details the “Row Erase” command and parameter P10 is shown in Figure 3-6.

Note 1: If the last row of program memory is erased, bit 3 of CONFIG1H must also be programmed as ‘0’.

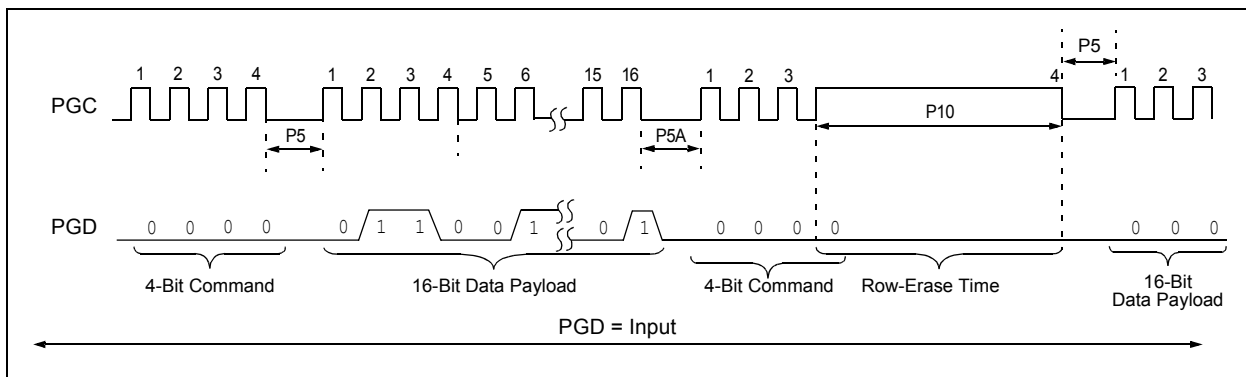
2: The TBLPTR register can point at any byte within the row intended for erase.

3: If code protection has been enabled, ICSP Bulk Erase (all program memory erased) operations can be used to disable code protection. ICSP Row Erase operations cannot be used to disable code protection.

TABLE 3-2: ERASE CODE MEMORY CODE SEQUENCE

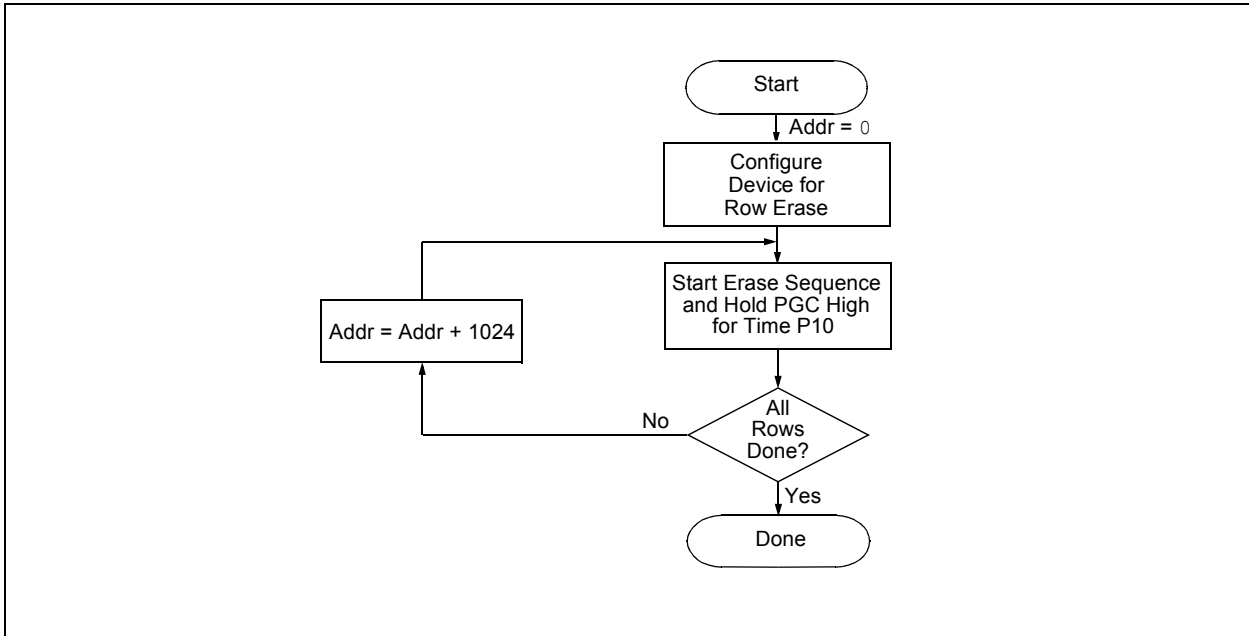
| 4-Bit Command | Data Payload | Core Instruction |
|---|--------------|-----------------------------------|
| Step 1: Enable memory writes. | | |
| 0000 | 84 A6 | BSF EECON1, WREN |
| Step 2: Point to first row in code memory. | | |
| 0000 | 6A F8 | CLRF TBLPTRU |
| 0000 | 6A F7 | CLRF TBLPTRH |
| 0000 | 6A F6 | CLRF TBLPTRL |
| Step 3: Enable erase and erase single row. | | |
| 0000 | 88 A6 | BSF EECON1, FREE |
| 0000 | 82 A6 | BSF EECON1, WR |
| 0000 | 00 00 | NOP - hold PGC high for time P10. |
| Step 4: Repeat step 3, with Address Pointer incremented by 1024, until all rows are erased. | | |

FIGURE 3-3: SET WR AND START ROW ERASE TIMING



PIC18F2XJXX/4XJXX FAMILY

FIGURE 3-4: SINGLE ROW ERASE CODE MEMORY FLOW



PIC18F2XJXX/4XJXX FAMILY

3.2 Code Memory Programming

Programming code memory is accomplished by first loading data into the write buffer and then initiating a programming sequence. The write buffer for all devices in the PIC18F2XJXX/4XJXX family is 64 bytes. It can be mapped to any 64-byte block beginning at 000000h. The actual memory write sequence takes the contents of this buffer and programs the 64-byte block of code memory indicated by the Table Pointer.

Write buffer locations are not cleared following a write operation; the buffer retains its data after the write is complete. This means that the buffer must be written with 64 bytes on each operation. If there are locations in the code memory that are to remain empty, the corresponding locations in the buffer must be filled with FFFFh. This avoids rewriting old data from the previous cycle.

The programming duration is internally timed. After a Start Programming command is issued (4-bit command, '1111'), a NOP is issued, where the 4th PGC is held high for the duration of the programming time, P9.

The code sequence to program a PIC18F2XJXX/4XJXX family device is shown in Table 3-3. The flowchart shown in Figure 3-5 depicts the logic necessary to completely write a PIC18F2XJXX/4XJXX family device. The timing diagram that details the Start Programming command and parameter P9 is shown in Figure 3-6.

Note 1: The TBLPTR register must point to the same region when initiating the programming sequence as it did when the write buffers were loaded.

TABLE 3-3: WRITE CODE MEMORY CODE SEQUENCE

| 4-Bit Command | Data Payload | Core Instruction |
|--|------------------|--|
| Step 1: Enable writes. | | |
| 0000 | 84 A6 | BSF EECON1, WREN |
| Step 2: Load write buffer. | | |
| 0000 | 0E <Addr[21:16]> | MOVLW <Addr[21:16]> |
| 0000 | 6E F8 | MOVWF TBLPTRU |
| 0000 | 0E <Addr[15:8]> | MOVLW <Addr[15:8]> |
| 0000 | 6E F7 | MOVWF TBLPTRH |
| 0000 | 0E <Addr[7:0]> | MOVLW <Addr[7:0]> |
| 0000 | 6E F6 | MOVWF TBLPTRL |
| Step 3: Repeat for all but the last two bytes. Any unused locations should be filled with FFFFh. | | |
| 1101 | <MSB><LSB> | Write 2 bytes and post-increment address by 2. |
| Step 4: Load write buffer for last two bytes. | | |
| 1111 | <MSB><LSB> | Write 2 bytes and start programming. |
| 0000 | 00 00 | NOP - hold PGC high for time P9. |
| To continue writing data, repeat steps 2 through 4, where the Address Pointer is incremented by 2 at each iteration of the loop. | | |

PIC18F2XJXX/4XJXX FAMILY

FIGURE 3-5: PROGRAM CODE MEMORY FLOW

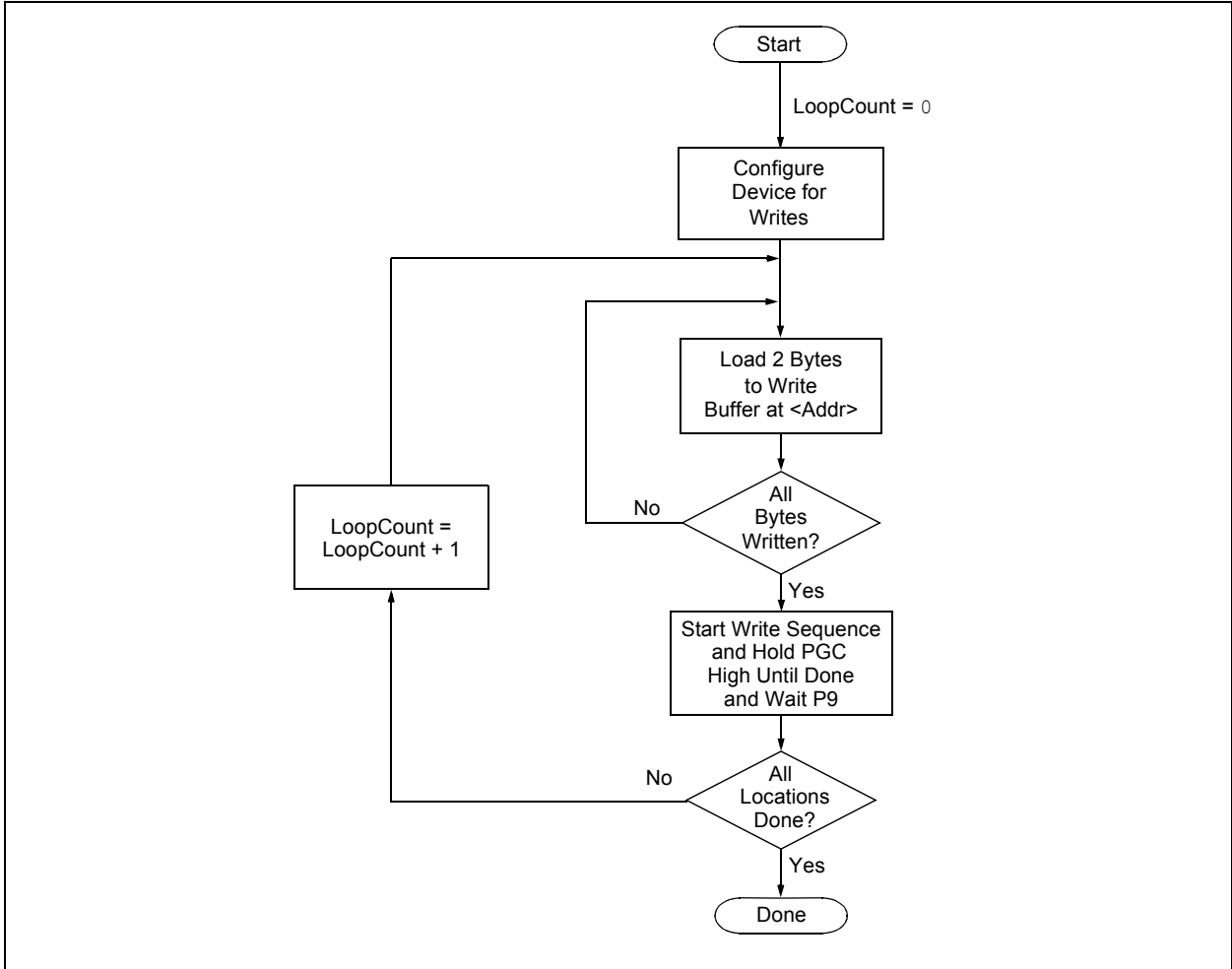
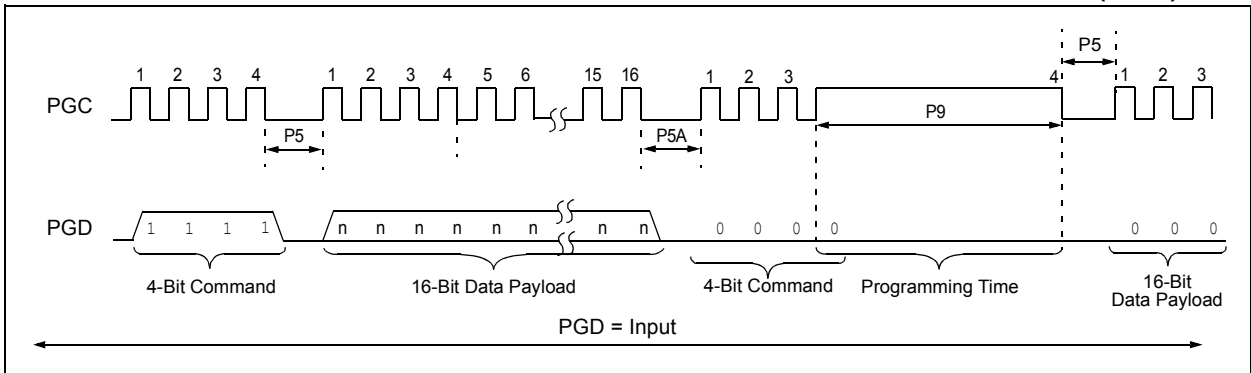


FIGURE 3-6: TABLE WRITE AND START PROGRAMMING INSTRUCTION TIMING (1111)



PIC18F2XJXX/4XJXX FAMILY

3.2.1 MODIFYING CODE MEMORY

The previous programming example assumed that the device had been Bulk Erased prior to programming. It may be the case, however, that the user wishes to modify only a section of an already programmed device.

The appropriate number of bytes required for the erase buffer must be read out of code memory (as described in **Section 4.2 “Verify Code Memory and Configuration Word”**) and buffered. Modifications can be made on this buffer. Then, the block of code memory that was read out must be erased and rewritten with the modified data. The code sequence is shown in Table 3-4.

The WREN bit must be set if the WR bit in EECON1 is used to initiate a write sequence.

3.2.2 CONFIGURATION WORD PROGRAMMING

Since the Flash Configuration Words are stored in program memory, they are programmed as if they were program data. Refer to **Section 3.2 “Code Memory Programming”** and **Section 3.2.1 “Modifying Code Memory”** for methods and examples on programming or modifying program memory. See also **Section 5.0 “Configuration Word”** for additional information on the Configuration Words.

TABLE 3-4: MODIFYING CODE MEMORY

| 4-Bit Command | Data Payload | Core Instruction |
|---|------------------|---|
| Step 1: Set the Table Pointer for the block to be erased. | | |
| 0000 | 0E <Addr[21:16]> | MOVLW <Addr[21:16]> |
| 0000 | 6E F8 | MOVWF TBLPTRU |
| 0000 | 0E <Addr[8:15]> | MOVLW <Addr[8:15]> |
| 0000 | 6E F7 | MOVWF TBLPTRH |
| 0000 | 0E <Addr[7:0]> | MOVLW <Addr[7:0]> |
| 0000 | 6E F6 | MOVWF TBLPTRL |
| Step 2: Read and modify code memory (see Section 4.1 “Read Code Memory”). | | |
| Step 3: Enable memory writes and set up an erase. | | |
| 0000 | 84 A6 | BSF EECON1, WREN |
| 0000 | 88 A6 | BSF EECON1, FREE |
| Step 4: Initiate erase. | | |
| 0000 | 82 A6 | BSF EECON1, WR |
| 0000 | 00 00 | NOP - hold PGC high for time P10. |
| Step 5: Load write buffer. The correct bytes will be selected based on the Table Pointer. | | |
| 0000 | 0E <Addr[21:16]> | MOVLW <Addr[21:16]> |
| 0000 | 6E F8 | MOVWF TBLPTRU |
| 0000 | 0E <Addr[8:15]> | MOVLW <Addr[8:15]> |
| 0000 | 6E F7 | MOVWF TBLPTRH |
| 0000 | 0E <Addr[7:0]> | MOVLW <Addr[7:0]> |
| 0000 | 6E F6 | MOVWF TBLPTRL |
| 1101 | <MSB><LSB> | Write 2 bytes and post-increment address by 2. |
| . | . | |
| . | . | Repeat write operation 30 more times to fill the write buffer |
| . | . | |
| 1111 | <MSB><LSB> | Write 2 bytes and start programming. |
| 0000 | 00 00 | NOP - hold PGC high for time P9. |
| Step 6: Repeat Step 5 for a total of 16 times (if rewriting the entire 1024 bytes of the erase page size). | | |
| Step 7: To continue modifying data, repeat Steps 1 through 5, where the Address Pointer is incremented by 1024 bytes at each iteration of the loop. | | |
| Step 8: Disable writes. | | |
| 0000 | 94 A6 | BCF EECON1, WREN |

3.3 Endurance and Retention

To maintain the endurance specification of the Flash program memory cells, each byte should never be programmed more than once between erase operations. Before attempting to modify the contents of a specific byte of Flash memory a second time, an erase operation (either a Bulk Erase or a Row Erase which includes that byte) should be performed.

PIC18F2XJXX/4XJXX FAMILY

4.0 READING THE DEVICE

4.1 Read Code Memory

Code memory is accessed one byte at a time via the 4-bit command, '1001' (table read, post-increment). The contents of memory pointed to by the Table Pointer (TBLPTRU:TBLPTRH:TBLPTRL) are serially output on PGD.

The 4-bit command is shifted in LSb first. The read is executed during the next 8 clocks, then shifted out on PGD during the last 8 clocks, LSb to MSb. A delay of

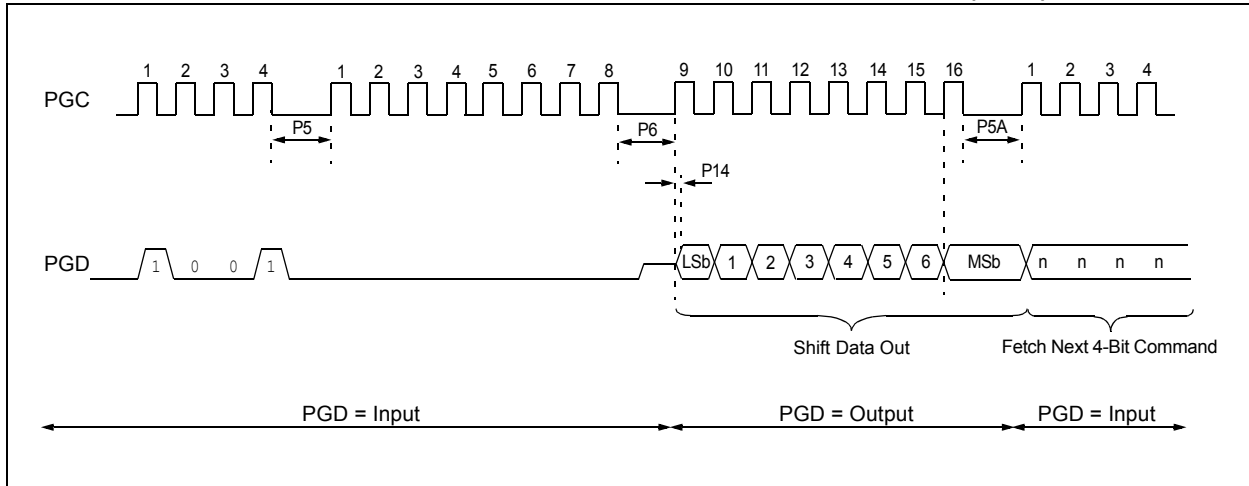
P6 must be introduced after the falling edge of the 8th PGC of the operand to allow PGD to transition from an input to an output. During this time, PGD must be held low (see Figure 4-1). This operation also increments the Table Pointer by one, pointing to the next byte in code memory for the next read.

This technique will work to read any memory in the 000000h to 3FFFFFFh address space, so it also applies to reading the Configuration registers.

TABLE 4-1: READ CODE MEMORY SEQUENCE

| 4-Bit Command | Data Payload | Core Instruction |
|--|------------------|--------------------|
| Step 1: Set Table Pointer. | | |
| 0000 | 0E <Addr[21:16]> | MOVLW Addr[21:16] |
| 0000 | 6E F8 | MOVWF TBLPTRU |
| 0000 | 0E <Addr[15:8]> | MOVLW <Addr[15:8]> |
| 0000 | 6E F7 | MOVWF TBLPTRH |
| 0000 | 0E <Addr[7:0]> | MOVLW <Addr[7:0]> |
| 0000 | 6E F6 | MOVWF TBLPTRL |
| Step 2: Read memory and then shift out on PGD, LSb to MSb. | | |
| 1001 | 00 00 | TBLRD *+ |

FIGURE 4-1: TABLE READ, POST-INCREMENT INSTRUCTION TIMING (1001)



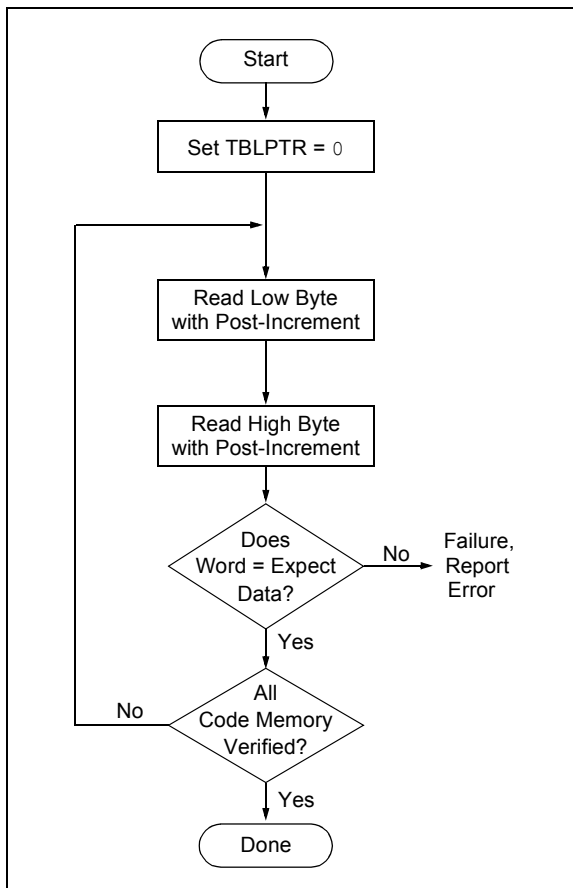
4.2 Verify Code Memory and Configuration Word

The verify step involves reading back the code memory space and comparing it against the copy held in the programmer's buffer. Because the Flash Configuration Words are stored at the end of program memory, it is verified with the rest of the code at this time.

The verify process is shown in the flowchart in Figure 4-2. Memory reads occur a single byte at a time, so two bytes must be read to compare against the word in the programmer's buffer. Refer to **Section 4.1 "Read Code Memory"** for implementation details of reading code memory.

Note: Because the Flash Configuration Word contains the device code protection bit, code memory should be verified immediately after writing if code protection is enabled. This is because the device will not be readable or verifiable if a device Reset occurs after the Flash Configuration Words (and the CP0 bit) have been cleared.

FIGURE 4-2: VERIFY CODE MEMORY FLOW



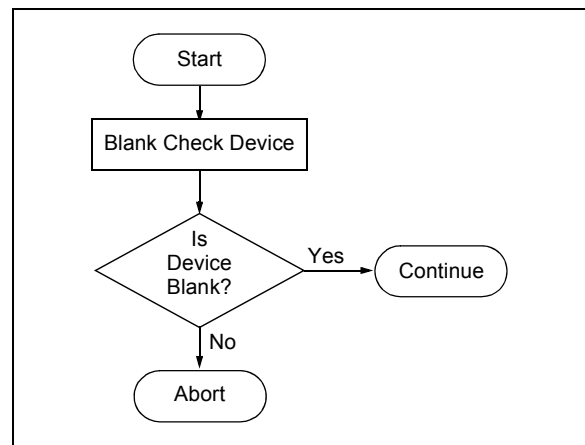
4.3 Blank Check

The term "Blank Check" means to verify that the device has no programmed memory cells. All memories must be verified: code memory and Configuration bits. The Device ID registers (3FFFFEh:3FFFFFh) should be ignored.

A "blank" or "erased" memory cell will read as a '1', so Blank Checking a device merely means to verify that all bytes read as FFh. The overall process flow is shown in Figure 4-3.

Given that Blank Checking is merely code verification with FFh expect data, refer to **Section 4.2 "Verify Code Memory and Configuration Word"** for implementation details.

FIGURE 4-3: BLANK CHECK FLOW



PIC18F2XJXX/4XJXX FAMILY

5.0 CONFIGURATION WORD

The Configuration Words of the PIC18F2XJXX/4XJXX family devices are implemented as volatile memory registers. All of the Configuration registers (CONFIG1L, CONFIG1H, CONFIG2L, CONFIG2H, CONFIG3L, CONFIG3H, CONFIG4L and CONFIG4H) are automatically loaded following each device Reset.

The data for these registers is taken from the four Flash Configuration Words located at the end of program memory. Configuration data is stored in order, starting with CONFIG1L in the lowest Flash address and ending with CONFIG4H in the highest. The mapping to specific Configuration Words is shown in Table 5-1. Users should always reserve these locations for Configuration Word data and write their application code accordingly.

The upper four bits of each Flash Configuration Word should always be stored in program memory as '1111'. This is done so these program memory addresses will always be '1111 xxxx xxxx xxxx' and interpreted as a NOP instruction if they were ever to be executed. Because the corresponding bits in the Configuration registers are unimplemented, they will not change the device's configuration.

The Configuration and Device ID registers are summarized in Table 5-2. A listing of the individual Configuration bits and their options is provided in Table 5-3.

TABLE 5-1: MAPPING OF THE FLASH CONFIGURATION WORDS TO THE CONFIGURATION REGISTERS

| Configuration Register | Flash Configuration Byte ⁽¹⁾ | Configuration Register Address |
|-------------------------|---|--------------------------------|
| CONFIG1L | XFF8h | 300000h |
| CONFIG1H | XFF9h | 300001h |
| CONFIG2L | XFFAh | 300002h |
| CONFIG2H | XFFBh | 300003h |
| CONFIG3L | XFFCh | 300004h |
| CONFIG3H | XFFDh | 300005h |
| CONFIG4L ⁽²⁾ | XFFEh | 300006h |
| CONFIG4H ⁽²⁾ | XFFFh | 300007h |

Note 1: See Table 2-2 for the complete addresses within code space for specific devices and memory sizes.

2: Unimplemented in PIC18F45J10 family devices.

TABLE 5-2: PIC18F45J10 FAMILY DEVICES: CONFIGURATION BITS AND DEVICE IDs

| File Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default/ Unprogrammed Value | |
|-----------|-----------------------|---------------------------|------------------|------------------|------------------|------------------|--------|--------|--------------------------------|-----------|
| 300000h | CONFIG1L | $\overline{\text{DEBUG}}$ | XINST | STVREN | — | — | — | — | WDTEN | 111- ---1 |
| 300001h | CONFIG1H | — ⁽¹⁾ | — ⁽¹⁾ | — ⁽¹⁾ | — ⁽¹⁾ | — ⁽²⁾ | CP0 | — | — | ---- 01-- |
| 300002h | CONFIG2L | IESO | FCMEN | — | — | — | FOSC2 | FOSC1 | FOSC0 | 11-- -111 |
| 300003h | CONFIG2H | — ⁽¹⁾ | — ⁽¹⁾ | — ⁽¹⁾ | — ⁽¹⁾ | WDTPS3 | WDTPS2 | WDTPS1 | WDTPS0 | ---- 1111 |
| 300005h | CONFIG3H | — ⁽¹⁾ | — ⁽¹⁾ | — ⁽¹⁾ | — ⁽¹⁾ | — | — | — | CCP2MX | ---- ---1 |
| 3FFFFEh | DEVID1 ⁽³⁾ | DEV2 | DEV1 | DEV0 | REV4 | REV3 | REV2 | REV1 | REV0 | See Table |
| 3FFFFFh | DEVID2 ⁽³⁾ | DEV10 | DEV9 | DEV8 | DEV7 | DEV6 | DEV5 | DEV4 | DEV3 | See Table |

Legend: — = unimplemented. Shaded cells are unimplemented, read as '0'.

Note 1: The value of these bits in program memory should always be '1'. This ensures that the location is executed as a NOP if it is accidentally executed.

2: This bit should always be maintained at '0'.

3: DEVID registers are read-only and cannot be programmed by the user.

PIC18F2XJXX/4XJXX FAMILY

TABLE 5-3: PIC18F45J10 FAMILY DEVICES: BIT DESCRIPTIONS

| Bit Name | Configuration Words | Description |
|------------|---------------------|---|
| DEBUG | CONFIG1L | Background Debugger Enable bit 1 = Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins 0 = Background debugger enabled, RB6 and RB7 are dedicated to in-circuit debug |
| XINST | CONFIG1L | Extended Instruction Set Enable bit 1 = Instruction set extension and Indexed Addressing mode enabled 0 = Instruction set extension and Indexed Addressing mode disabled (Legacy mode) |
| STVREN | CONFIG1L | Stack Overflow/Underflow Reset Enable bit 1 = Reset on stack overflow/underflow enabled 0 = Reset on stack overflow/underflow disabled |
| WDTEN | CONFIG1L | Watchdog Timer Enable bit 1 = WDT enabled 0 = WDT disabled (control is placed on SWDTEN bit) |
| CP0 | CONFIG1H | Code Protection bit 1 = Program memory is not code-protected 0 = Program memory is code-protected |
| IESO | CONFIG2L | Internal/External Oscillator Switchover bit 1 = Oscillator Switchover mode enabled 0 = Oscillator Switchover mode disabled |
| FCMEN | CONFIG2L | Fail-Safe Clock Monitor Enable bit 1 = Fail-Safe Clock Monitor enabled 0 = Fail-Safe Clock Monitor disabled |
| FOSC2 | CONFIG2L | Default Oscillator Select bit 1 = Clock designated by FOSC<1:0> is enabled as system clock when OSCCON<1:0> = 00 0 = INTRC is enabled as system clock when OSCCON<1:0> = 00 |
| FOSC<1:0> | CONFIG2L | Primary Oscillator Select bits 11 = EC oscillator, PLL enabled and under software control, CLKO function on OSC2 10 = EC oscillator, CLKO function on OSC2 01 = HS oscillator, PLL enabled and under software control 00 = HS oscillator |
| WDTPS<3:0> | CONFIG2H | Watchdog Timer Postscale Select bits 1111 = 1:32,768 1110 = 1:16,384 1101 = 1:8,192 1100 = 1:4,096 1011 = 1:2,048 1010 = 1:1,024 1001 = 1:512 1000 = 1:256 0111 = 1:128 0110 = 1:64 0101 = 1:32 0100 = 1:16 0011 = 1:8 0010 = 1:4 0001 = 1:2 0000 = 1:1 |
| CCP2MX | CONFIG3H | CCP2 MUX bit 1 = CCP2 is multiplexed with RC1 0 = CCP2 is multiplexed with RB3 |

PIC18F2XJXX/4XJXX FAMILY

TABLE 5-4: PIC18F46J11 AND PIC18F46J50 FAMILY DEVICES: CONFIGURATION BITS AND DEVICE IDS

| File Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default/ Unprogrammed Value ⁽¹⁾ |
|------------------|------------------|------------------|------------------|------------------|------------------------|------------------------|------------------------|-----------------------|--|
| 300000h CONFIG1L | DEBUG | XINST | STVREN | — | PLLDIV2 ⁽³⁾ | PLLDIV1 ⁽³⁾ | PLLDIV0 ⁽³⁾ | WDTEN | 111- 1111 |
| 300001h CONFIG1H | — ⁽²⁾ | — ⁽²⁾ | — ⁽²⁾ | — ⁽²⁾ | — ⁽⁴⁾ | CP0 | CPDIV1 ⁽³⁾ | CPDIV0 ⁽³⁾ | ---- 0111 |
| 300002h CONFIG2L | IESO | FCMEN | — | LPT1OSC | T1DIG | FOSC2 | FOSC1 | FOSC0 | 11-1 1111 |
| 300003h CONFIG2H | — ⁽²⁾ | — ⁽²⁾ | — ⁽²⁾ | — ⁽²⁾ | WDTPS3 | WDTPS2 | WDTPS1 | WDTPS0 | ---- 1111 |
| 300004h CONFIG3L | DSWDTPS3 | DSWDTPS2 | DSWDTPS1 | DSWDTPS0 | DSWDTEN | DSBOREN | RTCOSC | DSWDTOSC | 1111 1111 |
| 300005h CONFIG3H | — ⁽²⁾ | — ⁽²⁾ | — ⁽²⁾ | — ⁽²⁾ | MSSPMSK | — | — | IOL1WAY | ---- 1--1 |
| 300006h CONFIG4L | WPCFG | WPEND | WFPF5 | WFPF4 | WFPF3 | WFPF2 | WFPF1 | WFPF0 | 1111 1111 |
| 300007h CONFIG4H | — ⁽²⁾ | — ⁽²⁾ | — ⁽²⁾ | — ⁽²⁾ | — | — | — | WPDIS | ---- ---1 |
| 3FFFFEh DEVID1 | DEV2 | DEV1 | DEV0 | REV4 | REV3 | REV2 | REV1 | REV0 | xxxx xxxx |
| 3FFFFFh DEVID2 | DEV10 | DEV9 | DEV8 | DEV7 | DEV6 | DEV5 | DEV4 | DEV3 | 0100 00xx |

Legend: x = unknown, u = unchanged, - = unimplemented. Shaded cells are unimplemented, read as '0'.

Note 1: Values reflect the unprogrammed state as received from the factory and following Power-on Resets. In all other Reset states, the configuration bytes maintain their previously programmed states.

2: The value of these bits in program memory should always be '1'. This ensures that the location is executed as a NOP if it is accidentally executed.

3: These bits are not implemented in PIC18F46J11 family devices.

4: This bit should always be maintained at '0'.

TABLE 5-5: PIC18F46J11 AND PIC18F46J50 FAMILY DEVICES: BIT DESCRIPTIONS

| Bit Name | Configuration Words | Description |
|----------------------------|---------------------|---|
| DEBUG | CONFIG1L | Background Debugger Enable bit 1 = Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins 0 = Background debugger enabled, RB6 and RB7 are dedicated to in-circuit debug |
| XINST | CONFIG1L | Enhanced Instruction Set Enable bit 1 = Instruction set extension and Indexed Addressing mode enabled 0 = Instruction set extension and Indexed Addressing mode disabled (Legacy mode) |
| STVREN | CONFIG1L | Stack Overflow/Underflow Reset Enable bit 1 = Reset on stack overflow/underflow enabled 0 = Reset on stack overflow/underflow disabled |
| PLLDIV<2:0> ⁽³⁾ | CONFIG1L | PLL Input Divider bits Divider must be selected to provide a 4 MHz input into the 96 MHz PLL. 111 = No divide – oscillator used directly (4 MHz input) 110 = Oscillator divided by 2 (8 MHz input) 101 = Oscillator divided by 3 (12 MHz input) 100 = Oscillator divided by 4 (16 MHz input) 011 = Oscillator divided by 5 (20 MHz input) 010 = Oscillator divided by 6 (24 MHz input) 001 = Oscillator divided by 10 (40 MHz input) 000 = Oscillator divided by 12 (48 MHz input) |
| WDTEN | CONFIG1L | Watchdog Timer Enable bit 1 = WDT enabled 0 = WDT disabled (control is placed on SWDTEN bit) |
| CP0 ⁽⁴⁾ | CONFIG1H | Code Protection bit 1 = Program memory is not code-protected 0 = Program memory is code-protected |

Note 1: The Configuration bits can only be programmed indirectly by programming the Flash Configuration Word.

2: The Configuration bits are reset to '1' only on VDD Reset; it is reloaded with the programmed value at any device Reset.

3: These bits are not implemented in PIC18F46J11 family devices.

4: Once this bit is cleared, all the Configuration registers which reside in the last page are also protected. To disable code protection, perform an ICSP™ Bulk Erase operation.

PIC18F2XJXX/4XJXX FAMILY

TABLE 5-5: PIC18F46J11 AND PIC18F46J50 FAMILY DEVICES: BIT DESCRIPTIONS (CONTINUED)

| Bit Name | Configuration Words | Description |
|---------------------------|---------------------------|--|
| CPDIV<1:0> ⁽³⁾ | CONFIG1H | CPU System Clock Selection bits 11 = No CPU system clock divide 10 = CPU system clock divided by 2 01 = CPU system clock divided by 3 00 = CPU system clock divided by 6 |
| IESO | CONFIG2L ^(1,2) | Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit 1 = Oscillator Switchover mode enabled 0 = Oscillator Switchover mode disabled |
| FCMEN | CONFIG2L ^(1,2) | Fail-Safe Clock Monitor Enable bit 1 = Fail-Safe Clock Monitor enabled 0 = Fail-Safe Clock Monitor disabled |
| LPT1OSC | CONFIG2L ^(1,2) | Low-Power Timer1 Oscillator Enable bit 1 = Timer1 oscillator configured for low-power operation 0 = Timer1 oscillator configured for higher power operation |
| T1DIG | CONFIG2L ^(1,2) | Secondary Clock Source T1OSCEN Enforcement bit ⁽¹⁾ 1 = Secondary oscillator clock source may be selected (OSCCON <1:0> = 01) regardless of T1OSCEN state 0 = Secondary oscillator clock source may not be selected unless T1CON <3> = 1 |
| FOSC<2:0> | CONFIG2L ^(1,2) | Oscillator Selection bits 111 = EC+PLL (S/W controlled by PLEN bit), CLKO on RA6 110 = EC oscillator (PLL always disabled) with CLKO on RA6 101 = HS+PLL (S/W controlled by PLEN bit) 100 = HS oscillator (PLL always disabled) 011 = INTOSCPLLO, internal oscillator with PLL (S/W controlled by PLEN bit), CLKO on RA6, port function on RA7 010 = INTOSCPPL, internal oscillator with PLL (S/W controlled by PLEN bit), port function on RA6 and RA7 001 = INTOSCO, internal oscillator, INTOSC or INTRC (PLL always disabled), CLKO on RA6, port function on RA7 000 = INTOSC, internal oscillator INTOSC or INTRC (PLL always disabled), port function on RA6 and RA7 |
| WDTPS<3:0> | CONFIG2H ^(1,2) | Watchdog Timer Postscale Select bits 1111 = 1:32,768 1110 = 1:16,384 1101 = 1:8,192 1100 = 1:4,096 1011 = 1:2,048 1010 = 1:1,024 1001 = 1:512 1000 = 1:256 0111 = 1:128 0110 = 1:64 0101 = 1:32 0100 = 1:16 0011 = 1:8 0010 = 1:4 0001 = 1:2 0000 = 1:1 |

- Note 1:** The Configuration bits can only be programmed indirectly by programming the Flash Configuration Word.
Note 2: The Configuration bits are reset to '1' only on VDD Reset; it is reloaded with the programmed value at any device Reset.
Note 3: These bits are not implemented in PIC18F46J11 family devices.
Note 4: Once this bit is cleared, all the Configuration registers which reside in the last page are also protected. To disable code protection, perform an ICSP™ Bulk Erase operation.

PIC18F2XJXX/4XJXX FAMILY

TABLE 5-5: PIC18F46J11 AND PIC18F46J50 FAMILY DEVICES: BIT DESCRIPTIONS (CONTINUED)

| Bit Name | Configuration Words | Description |
|--------------------------|---------------------|--|
| DSWTPS<3:0> | CONFIG3L | Deep Sleep Watchdog Timer Postscale Select bits The DSWDT prescaler is 32; this creates an approximate base time unit of 1 ms. 1111 = 1:2,147,483,648 (25.7 days) 1110 = 1:536,870,912 (6.4 days) 1101 = 1:134,217,728 (38.5 hours) 1100 = 1:33,554,432 (9.6 hours) 1011 = 1:8,388,608 (2.4 hours) 1010 = 1:2,097,152 (36 minutes) 1001 = 1:524,288 (9 minutes) 1000 = 1:131,072 (135 seconds) 0111 = 1:32,768 (34 seconds) 0110 = 1:8,192 (8.5 seconds) 0101 = 1:2,048 (2.1 seconds) 0100 = 1:512 (528 ms) 0011 = 1:128 (132 ms) 0010 = 1:32 (33 ms) 0001 = 1:8 (8.3 ms) 0000 = 1:2 (2.1 ms) |
| DSWDTEN | CONFIG3L | Deep Sleep Watchdog Timer Enable bit 1 = DSWDT enabled 0 = DSWDT disabled |
| DSBOREN | CONFIG3L | Deep Sleep BOR Enable bit 1 = BOR enabled in Deep Sleep 0 = BOR disabled in Deep Sleep (does not affect operation in non Deep Sleep modes) |
| RTCOSC | CONFIG3L | RTCC Reference Clock Select bit 1 = RTCC uses T1OSC/T1CKI as reference clock 0 = RTCC uses INTRC as reference clock |
| DSWDTOSC | CONFIG3L | DSWDT Reference Clock Select bit 1 = DSWDT uses INTRC as reference clock 0 = DSWDT uses T1OSC/T1CKI as reference clock |
| MSSPMSK ^(1,2) | CONFIG3H | MSSP 7-Bit Address Masking Mode Enable bit 1 = 7-Bit Address Masking mode enable 0 = 5-Bit Address Masking mode enable |
| IOL1WAY | CONFIG3H | IOLOCK Bit One-Way Set Enable bit 1 = The IOLOCK bit (PPSCON<0>) can be set once, provided the unlock sequence has been completed. Once set, the Peripheral Pin Select registers cannot be written to a second time. 0 = The IOLOCK bit (PPSCON<0>) can be set and cleared as needed, provided the unlock sequence has been completed |
| WPCFG ⁽⁴⁾ | CONFIG4L | Write/Erase Protect Configuration Words Page bit (valid when WPDIS = 0) 1 = Configuration Words page is not erase/write-protected unless WPEND and WPPF<5:0> settings include the Configuration Words page 0 = Configuration Words page is erase/write-protected, regardless of WPEND and WPPF<5:0> settings |
| WPEND | CONFIG4L | Write/Erase Protect Region Select bit (valid when WPDIS = 0) 1 = Flash pages, WPPF<5:0> to Configuration Words page, are write/erase-protected 0 = Flash pages, 0 to WPPF<5:0> are write/erase-protected |

- Note 1:** The Configuration bits can only be programmed indirectly by programming the Flash Configuration Word.
Note 2: The Configuration bits are reset to '1' only on VDD Reset; it is reloaded with the programmed value at any device Reset.
Note 3: These bits are not implemented in PIC18F46J11 family devices.
Note 4: Once this bit is cleared, all the Configuration registers which reside in the last page are also protected. To disable code protection, perform an ICSP™ Bulk Erase operation.

PIC18F2XJXX/4XJXX FAMILY

TABLE 5-5: PIC18F46J11 AND PIC18F46J50 FAMILY DEVICES: BIT DESCRIPTIONS (CONTINUED)

| Bit Name | Configuration Words | Description |
|----------------------|---------------------|---|
| WFPF<5:0> | CONFIG4L | Write/Erase Protect Page Start/End Location bits Used with WPEND bit to define which pages in Flash will be write/erase-protected. |
| WPDIS ⁽⁵⁾ | CONFIG4H | Write Protect Disable bit 1 = WFPF<5:0>, WPEND and WPCFG bits ignored; all Flash memory may be erased or written 0 = WFPF<5:0>, WPEND and WPCFG bits enabled; write/erase-protect active for the selected region(s) |
| DEV<2:0> | DEVID1 | Device ID bits Used with the DEV<10:3> bits in the Device ID Register 2 to identify the part number. |
| REV<4:0> | DEVID1 | Revision ID bits Indicate the device revision. |
| DEV<10:3> | DEVID2 | Device ID bits Used with the DEV<2:0> bits in the Device ID Register 1 to identify the part number. |

- Note 1:** The Configuration bits can only be programmed indirectly by programming the Flash Configuration Word.
Note 2: The Configuration bits are reset to '1' only on VDD Reset; it is reloaded with the programmed value at any device Reset.
Note 3: These bits are not implemented in PIC18F46J11 family devices.
Note 4: Once this bit is cleared, all the Configuration registers which reside in the last page are also protected. To disable code protection, perform an ICSP™ Bulk Erase operation.

TABLE 5-6: PIC18F47J13 AND PIC18F47J53 FAMILY DEVICES: CONFIGURATION BITS AND DEVICE IDs

| File Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Default/ Unprogrammed Value ⁽¹⁾ | |
|-----------|----------|----------|----------|----------|----------|------------------------|---------|-----------------------|--|-----------|
| 300000h | CONFIG1L | DEBUG | XINST | STVREN | CFGPLLEN | PLLDIV2 | PLLDIV1 | PLLDIV0 | WDTEN | 111- 1111 |
| 300001h | CONFIG1H | _(2) | _(2) | _(2) | _(2) | _(4) | CP0 | CPDIV1 ⁽³⁾ | CPDIV0 ⁽³⁾ | ---- 0111 |
| 300002h | CONFIG2L | IESO | FCMEN | CLKOEC | SOSCSEL1 | SOSCSEL0 | FOSC2 | FOSC1 | FOSC0 | 1111 1111 |
| 300003h | CONFIG2H | _(2) | _(2) | _(2) | _(2) | WDTPS3 | WDTPS2 | WDTPS1 | WDTPS0 | ---- 1111 |
| 300004h | CONFIG3L | DSWDTPS3 | DSWDTPS2 | DSWDTPS1 | DSWDTPS0 | DSWDTEN | DSBOREN | RTCOSC | DSWDTOSC | 1111 1111 |
| 300005h | CONFIG3H | _(2) | _(2) | _(2) | _(2) | MSSPMSK | PLLSEL | ADCSEL | IOL1WAY | ---- 1111 |
| 300006h | CONFIG4L | WPCFG | WFPF6 | WFPF5 | WFPF4 | WFPF3 | WFPF2 | WFPF1 | WFPF0 | 1111 1111 |
| 300007h | CONFIG4H | _(2) | _(2) | _(2) | _(2) | LS48MHZ ⁽³⁾ | — | WPEND | WPDIS | ---- 1-11 |
| 3FFFFEh | DEVID1 | DEV2 | DEV1 | DEV0 | REV4 | REV3 | REV2 | REV1 | REV0 | xxxx xxxx |
| 3FFFFFh | DEVID2 | DEV10 | DEV9 | DEV8 | DEV7 | DEV6 | DEV5 | DEV4 | DEV3 | 0101 10xx |

- Legend:** x = unknown, u = unchanged, - = unimplemented. Shaded cells are unimplemented, read as '0'.
Note 1: Values reflect the unprogrammed state as received from the factory and following Power-on Resets. In all other Reset states, the configuration bytes maintain their previously programmed states.
Note 2: The value of these bits in program memory should always be '1'. This ensures that the location is executed as a NOP if it is accidentally executed.
Note 3: These bits are not implemented in PIC18F47J13 family devices.
Note 4: This bit should always be maintained at '0'.

PIC18F2XJXX/4XJXX FAMILY

TABLE 5-7: PIC18F47J13 AND PIC18F47J53 FAMILY DEVICES: BIT DESCRIPTIONS

| Bit Name | Configuration Words | Description |
|---------------------------|---------------------------|--|
| DEBUG | CONFIG1L | Background Debugger Enable bit 1 = Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins 0 = Background debugger enabled, RB6 and RB7 are dedicated to in-circuit debug |
| XINST | CONFIG1L | Enhanced Instruction Set Enable bit 1 = Instruction set extension and Indexed Addressing mode enabled 0 = Instruction set extension and Indexed Addressing mode disabled (Legacy mode) |
| STVREN | CONFIG1L | Stack Overflow/Underflow Reset Enable bit 1 = Reset on stack overflow/underflow enabled 0 = Reset on stack overflow/underflow disabled |
| CFGPLEN | CONFIG1L | Enable PLL on Start-up bit 1 = PLL enabled on start-up. Not recommended for low-voltage designs. 0 = PLL disabled on start-up. Firmware may later enable PLL through OSCTUNE<6>. |
| PLLDIV<2:0> | CONFIG1L | 96 MHz PLL Input Divider bits Divider must be selected to provide a 4 MHz input into the 96 MHz PLL. 111 = No divide – oscillator used directly (4 MHz input) 110 = Oscillator divided by 2 (8 MHz input) 101 = Oscillator divided by 3 (12 MHz input) 100 = Oscillator divided by 4 (16 MHz input) 011 = Oscillator divided by 5 (20 MHz input) 010 = Oscillator divided by 6 (24 MHz input) 001 = Oscillator divided by 10 (40 MHz input) 000 = Oscillator divided by 12 (48 MHz input) |
| WDTEN | CONFIG1L | Watchdog Timer Enable bit 1 = WDT enabled 0 = WDT disabled (control is placed on SWDTEN bit) |
| CP0 ⁽⁴⁾ | CONFIG1H | Code Protection bit 1 = Program memory is not code-protected 0 = Program memory is code-protected |
| CPDIV<1:0> ⁽³⁾ | CONFIG1H | CPU System Clock Selection bits 11 = No CPU system clock divide 10 = CPU system clock divided by 2 01 = CPU system clock divided by 3 00 = CPU system clock divided by 6 |
| IESO | CONFIG2L ^(1,2) | Two-Speed Start-up (Internal/External Oscillator Switchover) Control bit 1 = Oscillator Switchover mode enabled 0 = Oscillator Switchover mode disabled |
| FCMEN | CONFIG2L ^(1,2) | Fail-Safe Clock Monitor Enable bit 1 = Fail-Safe Clock Monitor enabled 0 = Fail-Safe Clock Monitor disabled |
| CLKOEC | CONFIG2L | EC Mode Clock Output Enable bit 1 = CLKO output signal active on the RA6 pin (EC mode only) 0 = CLKO output disabled |
| SOSCSEL<1:0> | CONFIG2L | Secondary Oscillator Circuit Selection bits 11 = High-power SOSC circuit selected 10 = Digital Input mode (SCLKI) 01 = Low-power SOSC circuit selected 00 = Reserved |

- Note 1:** The Configuration bits can only be programmed indirectly by programming the Flash Configuration Word.
Note 2: The Configuration bits are reset to '1' only on VDD Reset; it is reloaded with the programmed value at any device Reset.
Note 3: These bits are not implemented in PIC18F47J13 family devices.
Note 4: Once this bit is cleared, all the Configuration registers which reside in the last page are also protected. To disable code protection, perform an ICSP™ Bulk Erase operation.
Note 5: Not implemented on PIC18F47J53 family devices.

PIC18F2XJXX/4XJXX FAMILY

TABLE 5-7: PIC18F47J13 AND PIC18F47J53 FAMILY DEVICES: BIT DESCRIPTIONS (CONTINUED)

| Bit Name | Configuration Words | Description |
|-------------|---------------------------|---|
| FOSC<2:0> | CONFIG2L ^(1,2) | <p>Oscillator Selection bits</p> <p>111 = EC+PLL (S/W controlled by PLEN bit), CLKO on RA6</p> <p>110 = EC oscillator (PLL always disabled) with CLKO on RA6</p> <p>101 = HS+PLL (S/W controlled by PLEN bit)</p> <p>100 = HS oscillator (PLL always disabled)</p> <p>011 = INTOSCPLLO, internal oscillator with PLL (S/W controlled by PLEN bit), CLKO on RA6, port function on RA7</p> <p>010 = INTOSCPLL, internal oscillator with PLL (S/W controlled by PLEN bit), port function on RA6 and RA7</p> <p>001 = INTOSCO, internal oscillator, INTOSC or INTRC (PLL always disabled), CLKO on RA6, port function on RA7</p> <p>000 = INTOSC, internal oscillator INTOSC or INTRC (PLL always disabled), port function on RA6 and RA7</p> |
| WDTPS<3:0> | CONFIG2H ^(1,2) | <p>Watchdog Timer Postscale Select bits</p> <p>1111 = 1:32,768</p> <p>1110 = 1:16,384</p> <p>1101 = 1:8,192</p> <p>1100 = 1:4,096</p> <p>1011 = 1:2,048</p> <p>1010 = 1:1,024</p> <p>1001 = 1:512</p> <p>1000 = 1:256</p> <p>0111 = 1:128</p> <p>0110 = 1:64</p> <p>0101 = 1:32</p> <p>0100 = 1:16</p> <p>0011 = 1:8</p> <p>0010 = 1:4</p> <p>0001 = 1:2</p> <p>0000 = 1:1</p> |
| DSWTPS<3:0> | CONFIG3L | <p>Deep Sleep Watchdog Timer Postscale Select bits</p> <p>The DSWDT prescaler is 32; this creates an approximate base time unit of 1 ms.</p> <p>1111 = 1:2,147,483,648 (25.7 days)</p> <p>1110 = 1:536,870,912 (6.4 days)</p> <p>1101 = 1:134,217,728 (38.5 hours)</p> <p>1100 = 1:33,554,432 (9.6 hours)</p> <p>1011 = 1:8,388,608 (2.4 hours)</p> <p>1010 = 1:2,097,152 (36 minutes)</p> <p>1001 = 1:524,288 (9 minutes)</p> <p>1000 = 1:131,072 (135 seconds)</p> <p>0111 = 1:32,768 (34 seconds)</p> <p>0110 = 1:8,192 (8.5 seconds)</p> <p>0101 = 1:2,048 (2.1 seconds)</p> <p>0100 = 1:512 (528 ms)</p> <p>0011 = 1:128 (132 ms)</p> <p>0010 = 1:32 (33 ms)</p> <p>0001 = 1:8 (8.3 ms)</p> <p>0000 = 1:2 (2.1 ms)</p> |
| DSWDTEN | CONFIG3L | <p>Deep Sleep Watchdog Timer Enable bit</p> <p>1 = DSWDT enabled</p> <p>0 = DSWDT disabled</p> |
| DSBOREN | CONFIG3L | <p>Deep Sleep BOR Enable bit</p> <p>1 = BOR enabled in Deep Sleep</p> <p>0 = BOR disabled in Deep Sleep (does not affect operation in non Deep Sleep modes)</p> |

- Note 1:** The Configuration bits can only be programmed indirectly by programming the Flash Configuration Word.
- Note 2:** The Configuration bits are reset to '1' only on VDD Reset; it is reloaded with the programmed value at any device Reset.
- Note 3:** These bits are not implemented in PIC18F47J13 family devices.
- Note 4:** Once this bit is cleared, all the Configuration registers which reside in the last page are also protected. To disable code protection, perform an ICSP™ Bulk Erase operation.
- Note 5:** Not implemented on PIC18F47J53 family devices.

PIC18F2XJXX/4XJXX FAMILY

TABLE 5-7: PIC18F47J13 AND PIC18F47J53 FAMILY DEVICES: BIT DESCRIPTIONS (CONTINUED)

| Bit Name | Configuration Words | Description |
|--------------------------|---------------------|---|
| RTCOSC | CONFIG3L | RTCC Reference Clock Select bit 1 = RTCC uses T1OSC/T1CKI as reference clock 0 = RTCC uses INTRC as reference clock |
| DSWDTOSC | CONFIG3L | DSWDT Reference Clock Select bit 1 = DSWDT uses INTRC as reference clock 0 = DSWDT uses T1OSC/T1CKI as reference clock |
| MSSPMSK ^(1,2) | CONFIG3H | MSSP 7-Bit Address Masking Mode Enable bit 1 = 7-Bit Address Masking mode enable 0 = 5-Bit Address Masking mode enable |
| PLLSEL ⁽⁵⁾ | CONFIG3H | PLL Selection bit 1 = 4x PLL selected 0 = 96 MHz PLL selected |
| ADCSEL | CONFIG3H | ADC Mode Selection bit 1 = 10-Bit ADC mode selected 0 = 12-Bit ADC mode selected |
| IOL1WAY | CONFIG3H | IOLOCK Bit One-Way Set Enable bit 1 = The IOLOCK bit (PPSCON<0>) can be set once, provided the unlock sequence has been completed. Once set, the Peripheral Pin Select registers cannot be written to a second time. 0 = The IOLOCK bit (PPSCON<0>) can be set and cleared as needed, provided the unlock sequence has been completed |
| WPCFG | CONFIG4L | Write/Erase Protect Configuration Words Page bit (valid when WPDIS = 0) 1 = Configuration Words page is not erase/write-protected unless WPEND and WPPF<6:0> settings include the Configuration Words page 0 = Configuration Words page is erase/write-protected, regardless of WPEND and WPPF<6:0> |
| WPPF<6:0> | CONFIG4L | Write/Erase Protect Page Start/End Location bits Used with WPEND bit to define which pages in Flash will be write/erase-protected. |
| WPEND | CONFIG4H | Write/Erase Protect Region Select bit (valid when WPDIS = 0) 1 = Flash pages, WPPF<6:0> to Configuration Words page, are write/erase-protected 0 = Flash pages, 0 to WPPF<6:0> are write/erase-protected |
| WPDIS | CONFIG4H | Write Protect Disable bit 1 = WPPF<6:0>, WPEND and WPCFG bits ignored; all Flash memory may be erased or written 0 = WPPF<6:0>, WPEND and WPCFG bits enabled; write/erase-protect active for the selected region(s) |
| LS48MHZ ⁽³⁾ | CONFIG4H | System Clock Selection bit 1 = System clock is expected at 48 MHz, FS/LS USB CLKEN's divide-by is set to 8 0 = System clock is expected at 24 MHz, FS/LS USB CLKEN's divide-by is set to 4 |
| DEV<2:0> | DEVID1 | Device ID bits Used with the DEV<10:3> bits in the Device ID Register 2 to identify the part number. |
| REV<4:0> | DEVID1 | Revision ID bits Indicate the device revision. |
| DEV<10:3> | DEVID2 | Device ID bits Used with the DEV<2:0> bits in the Device ID Register 1 to identify the part number. |

- Note 1:** The Configuration bits can only be programmed indirectly by programming the Flash Configuration Word.
Note 2: The Configuration bits are reset to '1' only on VDD Reset; it is reloaded with the programmed value at any device Reset.
Note 3: These bits are not implemented in PIC18F47J13 family devices.
Note 4: Once this bit is cleared, all the Configuration registers which reside in the last page are also protected. To disable code protection, perform an ICSP™ Bulk Erase operation.
Note 5: Not implemented on PIC18F47J53 family devices.

PIC18F2XJXX/4XJXX FAMILY

5.1 Device ID Word

The Device ID Word for the PIC18F2XJXX/4XJXX family devices is located at 3FFFEh:3FFFFh. These read-only bits may be used by the programmer to identify what device type is being programmed and read out normally, even after code protection has been enabled. The process for reading the device IDs is shown in Figure 5-1. A complete list of device ID values for the PIC18F2XJXX/4XJXX family is presented in Table 5-8.

FIGURE 5-1: READ DEVICE ID WORD FLOW

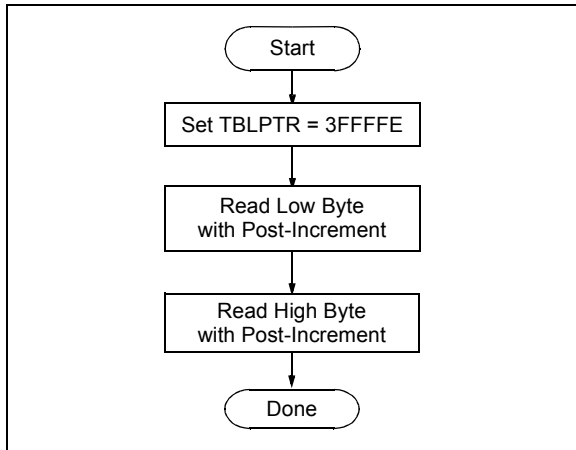


TABLE 5-8: DEVICE ID VALUE

| Device | Device ID Value | |
|--------------|-----------------|-----------|
| | DEVID2 | DEVID1 |
| PIC18F24J10 | 1Dh | 000x xxxx |
| PIC18F25J10 | 1Ch | 000x xxxx |
| PIC18F44J10 | 1Dh | 001x xxxx |
| PIC18F45J10 | 1Ch | 001x xxxx |
| PIC18LF24J10 | 1Dh | 010x xxxx |
| PIC18LF25J10 | 1Ch | 010x xxxx |
| PIC18LF44J10 | 1Dh | 011x xxxx |
| PIC18LF45J10 | 1Ch | 011x xxxx |
| PIC18F25J11 | 4Dh | 101x xxxx |
| PIC18F24J11 | 4Dh | 100x xxxx |
| PIC18F26J11 | 4Dh | 110x xxxx |
| PIC18F45J11 | 4Eh | 000x xxxx |
| PIC18F44J11 | 4Dh | 111x xxxx |
| PIC18F46J11 | 4Eh | 001x xxxx |
| PIC18F24J50 | 4Ch | 000x xxxx |
| PIC18F25J50 | 4Ch | 001x xxxx |
| PIC18F26J50 | 4Ch | 010x xxxx |
| PIC18F44J50 | 4Ch | 011x xxxx |
| PIC18F45J50 | 4Ch | 100x xxxx |

TABLE 5-8: DEVICE ID VALUE (CONTINUED)

| Device | Device ID Value | |
|--------------|-----------------|-----------|
| | DEVID2 | DEVID1 |
| PIC18F46J50 | 4Ch | 101x xxxx |
| PIC18LF2450 | 4Ch | 110x xxxx |
| PIC18LF25J50 | 4Ch | 111x xxxx |
| PIC18LF26J50 | 4Dh | 000x xxxx |
| PIC18LF44J50 | 4Dh | 001x xxxx |
| PIC18LF45J50 | 4Dh | 010x xxxx |
| PIC18LF46J50 | 4Dh | 011x xxxx |
| PIC18LF24J11 | 4Eh | 010x xxxx |
| PIC18LF25J11 | 4Eh | 011x xxxx |
| PIC18LF26J11 | 4Eh | 100x xxxx |
| PIC18LF44J11 | 4Eh | 101x xxxx |
| PIC18LF45J11 | 4Eh | 110x xxxx |
| PIC18LF46J11 | 4Eh | 111x xxxx |
| PIC18F26J13 | 59h | 001x xxxx |
| PIC18F27J13 | 59h | 011x xxxx |
| PIC18F46J13 | 59h | 101x xxxx |
| PIC18F47J13 | 59h | 111x xxxx |
| PIC18LF26J13 | 5Bh | 001x xxxx |
| PIC18LF27J13 | 5Bh | 011x xxxx |
| PIC18LF46J13 | 5Bh | 101x xxxx |
| PIC18LF47J13 | 5Bh | 111x xxxx |
| PIC18F26J53 | 58h | 001x xxxx |
| PIC18F27J53 | 58h | 011x xxxx |
| PIC18F46J53 | 58h | 101x xxxx |
| PIC18F47J53 | 58h | 111x xxxx |
| PIC18LF26J53 | 5Ah | 001x xxxx |
| PIC18LF27J53 | 5Ah | 011x xxxx |
| PIC18LF46J53 | 5Ah | 101x xxxx |
| PIC18LF47J53 | 5Ah | 111x xxxx |

5.2 Checksum Computation

The checksum is calculated by summing the contents of all code memory locations and the device Configuration Words, appropriately masked. The Least Significant 16 bits of this sum are the checksum.

The checksum calculation differs depending on whether or not code protection is enabled. Since the code memory locations read out differently depending on the code-protect setting, the table describes how to manipulate the actual code memory values to simulate the values that would be read from a protected device. When calculating a checksum by reading a device, the entire code memory can simply be read and summed. The Configuration Words can always be read.

PIC18F2XJXX/4XJXX FAMILY

Table 5-9 describes how to calculate the checksum for each device.

TABLE 5-9: CHECKSUM COMPUTATION

| Device | Code Protection | Checksum |
|----------------------------|-----------------|--|
| PIC18F24J10 PIC18F44J10 | Off | SUM[000000:003FF7] + ([003FF8] & E1h) + ([003FF9] & 04h) + ([003FFA] & C7h) + ([003FFB] & 0Fh) + ([003FFD] & 01h) |
| | On | 0000h |
| PIC18F24J11 PIC18F44J11 | Off | SUM[000000:003FF7] + ([003FF8] & E1h) + ([003FF9] & FCh) + ([003FFA] & DFh) + ([003FFB] & FFh) + ([003FFC] & FFh) + ([003FFD] & F9h) + ([003FFE] & FFh) + ([003FFF] & F1h) |
| | On | 0000h |
| PIC18F24J50 PIC18F44J50 | Off | SUM[000000:003FF7] + ([003FF8] & EFh) + ([003FF9] & FFh) + ([003FFA] & DFh) + ([003FFB] & FFh) + ([003FFC] & FFh) + ([003FFD] & F9h) + ([003FFE] & FFh) + ([003FFF] & F1h) |
| | On | 0000h |
| PIC18F25J10 PIC18F45J10 | Off | SUM[000000:007FF7] + ([007FF8] & E1h) + ([007FF9] & 04h) + ([007FFA] & C7h) + ([007FFB] & 0Fh) + ([007FFD] & 01h) |
| | On | 0000h |
| PIC18F25J11 PIC18F45J11 | Off | SUM[000000:007FF7] + ([007FF8] & E1h) + ([007FF9] & FCh) + ([007FFA] & DFh) + ([007FFB] & FFh) + ([007FFC] & FFh) + ([007FFD] & F9h) + ([007FFE] & FFh) + ([007FFF] & F1h) |
| | On | 0000h |
| PIC18F25J50 PIC18F45J50 | Off | SUM[000000:007FF7] + ([007FF8] & EFh) + ([007FF9] & FFh) + ([007FFA] & DFh) + ([007FFB] & FFh) + ([007FFC] & FFh) + ([007FFD] & F9h) + ([007FFE] & FFh) + ([007FFF] & F1h) |
| | On | 0000h |
| PIC18F26J11 PIC18F46J11 | Off | SUM[000000:00FFF7] + ([00FFF8] & E1h) + ([00FFF9] & FCh) + ([00FFFA] & DFh) + ([00FFFB] & FFh) + ([00FFFC] & FFh) + ([00FFFD] & F9h) + ([00FFFE] & FFh) + ([00FFFF] & F1h) |
| | On | 0000h |
| PIC18F26J50 PIC18F46J50 | Off | SUM[000000:00FFF7] + ([00FFF8] & EFh) + ([00FFF9] & FFh) + ([00FFFA] & DFh) + ([00FFFB] & FFh) + ([00FFFC] & FFh) + ([00FFFD] & F9h) + ([00FFFE] & FFh) + ([00FFFF] & F1h) |
| | On | 0000h |
| PIC18F26J13 PIC18F46J13 | Off | SUM[000000:00FFF7] + ([00FFF8] & FFh) + ([00FFF9] & FCh) + ([00FFFA] & FFh) + ([00FFFB] & FFh) + ([00FFFC] & FFh) + ([00FFFD] & FFh) + ([00FFFE] & BFh) + ([00FFFF] & F3h) |
| | On | 0000h |
| PIC18F26J53 PIC18F46J53 | Off | SUM[000000:00FFF7] + ([00FFF8] & FFh) + ([00FFF9] & FFh) + ([00FFFA] & FFh) + ([00FFFB] & FFh) + ([00FFFC] & FFh) + ([00FFFD] & FBh) + ([00FFFE] & BFh) + ([00FFFF] & FBh) |
| | On | 0000h |
| PIC18F27J13 PIC18F47J13 | Off | SUM[000000:01FFF7] + ([01FFF8] & FFh) + ([01FFF9] & FCh) + ([01FFFA] & FFh) + ([01FFFB] & FFh) + ([01FFFC] & FFh) + ([01FFFD] & FFh) + ([01FFFE] & FFh) + ([01FFFF] & F3h) |
| | On | 0000h |
| PIC18F27J53 PIC18F47J53 | Off | SUM[000000:01FFF7] + ([01FFF8] & FFh) + ([01FFF9] & FFh) + ([01FFFA] & FFh) + ([01FFFB] & FFh) + ([01FFFC] & FFh) + ([01FFFD] & FBh) + ([01FFFE] & FFh) + ([01FFFF] & FBh) |
| | On | 0000h |

Legend: [a] = Value at address a; SUM[a:b] = Sum of locations a to b inclusive; + = Addition; & = Bitwise AND. All addresses are hexadecimal.

PIC18F2XJXX/4XJXX FAMILY

6.0 AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE

| Standard Operating Conditions | | | | | | | | |
|--|------------------|--|----------------------------|---------------------|-------|----------------------------------|-----------------------------|---|
| Operating Temperature: 25°C is recommended | | | | | | | | |
| Param No. | Symbol | Characteristic | Min | Max | Units | Conditions | | |
| | VDDCORE | External Supply Voltage for Microcontroller Core During Programming Operations (PIC18LF devices) | 2.25 | 2.75 | V | (Note 1) | | |
| D111 | VDD | Supply Voltage During Programming | PIC18LFXXJXX | VDDCORE | 3.60 | V | Normal programming (Note 2) | |
| | | | PIC18FXXJ10 | | 2.70 | 3.60 | | V |
| | | | PIC18FXXJ50 | | 2.35 | 3.60 | V | |
| | | | PIC18FXXJ11 | | | | | |
| | | | PIC18FXXJ53 PIC18FXXJ13 | | | | | |
| D112 | I _{PP} | Programming Current on $\overline{\text{MCLR}}$ | — | 5 | μA | | | |
| D113 | I _{DDP} | Supply Current During Programming | — | 10 | mA | | | |
| D031 | V _{IL} | Input Low Voltage | V _{SS} | 0.2 V _{DD} | V | | | |
| D041 | V _{IH} | Input High Voltage | 0.8 V _{DD} | V _{DD} | V | | | |
| D080 | V _{OL} | Output Low Voltage | — | 0.4 | V | I _{OL} = 3.4 mA @ 3.3V | | |
| D090 | V _{OH} | Output High Voltage | 2.4 | — | V | I _{OH} = -2.0 mA @ 3.3V | | |
| D012 | C _{IO} | Capacitive Loading on I/O pin (PGD) | — | 50 | pF | To meet AC specifications | | |
| | C _F | Filter Capacitor Value on V _{CAP} | PIC18LFXXJXX | 0.1 | — | μF | (Note 1) | |
| | | | PIC18FXXJ10 | 4.7 | 18 | μF | | |
| | | | PIC18FXXJ13 | 5.4 | 18 | μF | | |
| | | | PIC18FXXJ11 | | | | | |
| | | | PIC18FXXJ5X | | | | | |

Note 1: External power must be supplied to the VDDCORE/V_{CAP} pin if the on-chip voltage regulator is disabled. See Section 2.1.1 “PIC18F2XJXX/4XJXX/ LF2XJXX/LF4XJXX Devices and the On-Chip Voltage Regulator” for more information.

2: VDD must also be supplied to the AVDD pins during programming. AVDD and AVSS should always be within ±0.3V of VDD and VSS, respectively.

PIC18F2XJXX/4XJXX FAMILY

6.0 AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE (CONTINUED)

| Standard Operating Conditions | | | | | | |
|--|--------|--|-----|-----|-------|---|
| Operating Temperature: 25°C is recommended | | | | | | |
| Param No. | Symbol | Characteristic | Min | Max | Units | Conditions |
| P1 | TR | MCLR Rise Time to Enter Program/Verify mode | — | 1.0 | μs | |
| P2 | TPGC | Serial Clock (PGC) Period | 100 | — | ns | |
| P2A | TPGCL | Serial Clock (PGC) Low Time | 50 | — | ns | |
| P2B | TPGCH | Serial Clock (PGC) High Time | 50 | — | ns | |
| P3 | TSET1 | Input Data Setup Time to Serial Clock ↓ | 20 | — | ns | |
| P4 | THLD1 | Input Data Hold Time from PGC ↓ | 20 | — | ns | |
| P5 | TDLY1 | Delay Between 4-Bit Command and Command Operand | 50 | — | ns | |
| P5A | TDLY1A | Delay Between 4-Bit Command Operand and Next 4-Bit Command | 50 | — | ns | |
| P6 | TDLY2 | Delay Between Last PGC ↓ of Command Byte to First PGC ↑ of Read of Data Word | 20 | — | ns | |
| P9 | TDLY5 | Delay to allow Block Programming to Occur | 3.4 | — | ms | PIC18F2XJ10/PIC18F4XJ10 |
| | | | 1.2 | — | ms | PIC18F2XJ11/PIC18F4XJ11/ PIC18F2XJ13/PIC18F4XJ13/ PIC18F2XJ5X/PIC18F4XJ5X |
| P10 | TDLY6 | Delay to allow Row Erase to Occur | 49 | — | ms | PIC18F2XJ10/PIC18F4XJ10/ PIC18F2XJ13/PIC18F4XJ13/ PIC18F2XJ53/PIC18F4XJ53 |
| | | | 54 | — | ms | PIC18F2XJ11/PIC18F4XJ11/ PIC18F2XJ50/PIC18F4XJ50 |
| P11 | TDLY7 | Delay to allow Bulk Erase to Occur | 475 | — | ms | PIC18F2XJ10/PIC18F4XJ10/ PIC18F2XJ13/PIC18F4XJ13/ PIC18F2XJ53/PIC18F4XJ53 |
| | | | 524 | — | ms | PIC18F2XJ11/PIC18F4XJ11/ PIC18F2XJ50/PIC18F4XJ50 |
| P12 | THLD2 | Input Data Hold Time from MCLR ↑ | 400 | — | μs | |
| P13 | TSET2 | VDD ↑ Setup Time to MCLR ↑ | 100 | — | ns | |
| P14 | TVALID | Data Out Valid from PGC ↑ | 25 | — | ns | |
| P16 | TDLY8 | Delay Between Last PGC ↓ and MCLR ↓ | 20 | — | ns | |
| P17 | THLD3 | MCLR ↓ to VDD ↓ | 3 | — | μs | |
| P19 | TKEY1 | Delay from First MCLR ↓ to First PGC ↑ for Key Sequence on PGD | 4 | — | ms | |
| P20 | TKEY2 | Delay from Last PGC ↓ for Key Sequence on PGD to Second MCLR ↑ | 50 | — | ns | |

- Note 1:** External power must be supplied to the VDDCORE/VCAP pin if the on-chip voltage regulator is disabled. See **Section 2.1.1 “PIC18F2XJXX/4XJXX/ LF2XJXX/LF4XJXX Devices and the On-Chip Voltage Regulator”** for more information.
- 2:** VDD must also be supplied to the AVDD pins during programming. AVDD and AVSS should always be within ±0.3V of VDD and VSS, respectively.

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