BTA416Y-800B

3Q Hi-Com Triac

10 June 2014 Product data sheet

1. General description

Planar passivated high commutation three quadrant triac in a SOT78D (TO-220AB) internally insulated plastic package intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. This "series B" triac will commutate the full RMS current at the maximum rated junction temperature without the aid of a snubber. This device has high T_j operating capability and an internally isolated mounting base.

2. Features and benefits

- 3Q technology for improved noise immunity
- High commutation capability with maximum false trigger immunity
- High immunity to false turn-on by dV/dt
- High surge capability
- High $T_{j(max)}$
- Isolated mounting base with 2500 V (RMS) isolation
- Least sensitive gate for highest noise immunity
- Planar passivated for voltage ruggedness and reliability
- Triggering in three quadrants only
- Very high immunity to false turn-on by dV/dt

3. Applications

- Electronic thermostats (heating and cooling)
- High power motor controls
- Rectifier-fed DC inductive loads e.g. DC motors and solenoids

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	-	800	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; Fig. 4; Fig. 5		-	-	160	A
T_j	junction temperature			-	-	150	°C
$I_{T(RMS)}$	RMS on-state current	full sine wave; T_{mb} ≤ 108 °C; Fig. 1; Fig. 2; Fig. 3		-	-	16	A

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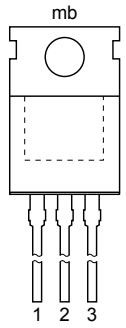
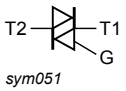
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 7		2	-	50	mA
		V_D = 12 V; I_T = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 7		2	-	50	mA
		V_D = 12 V; I_T = 0.1 A; T2- G-; T_j = 25 °C; Fig. 7		2	-	50	mA

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 **TO-220AB (SOT78D)**	 *sym051*
2	T2	main terminal 2		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

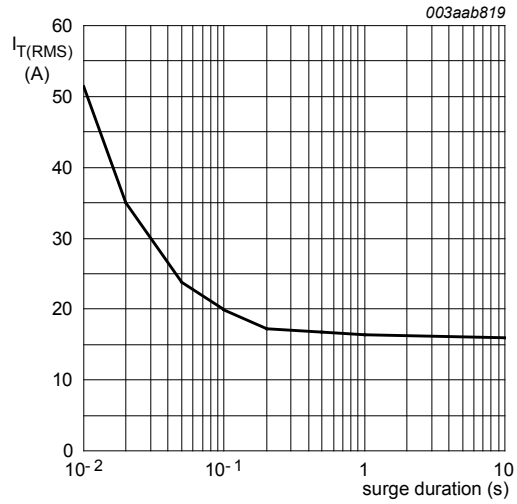
Type number	Package		
	Name	Description	Version
BTA416Y-800B	TO-220AB	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220	SOT78D

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 108$ °C; Fig. 1; Fig. 2; Fig. 3		-	16	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig. 4; Fig. 5		-	160	A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms		-	176	A
I^2t	I^2t for fusing	$t_p = 10$ ms; SIN		-	128	A^2s
dI_T/dt	rate of rise of on-state current	$I_T = 20$ A; $I_G = 0.2$ A; $dI_G/dt = 0.2$ A/µs		-	100	A/µs
I_{GM}	peak gate current			-	4	A
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	1	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	150	°C



f = 50 Hz; T_{mb} = 108 °C

Fig. 1. RMS on-state current as a function of surge duration; maximum values

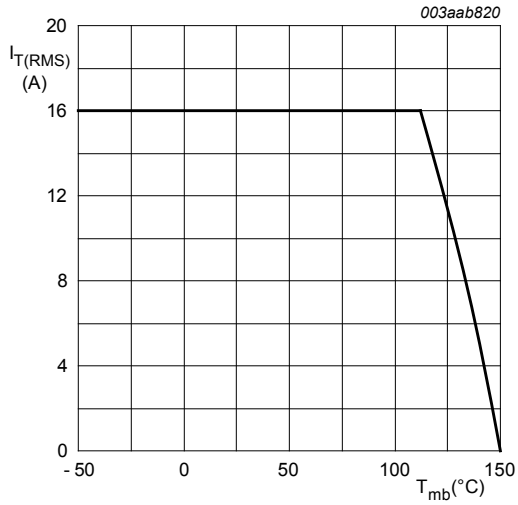
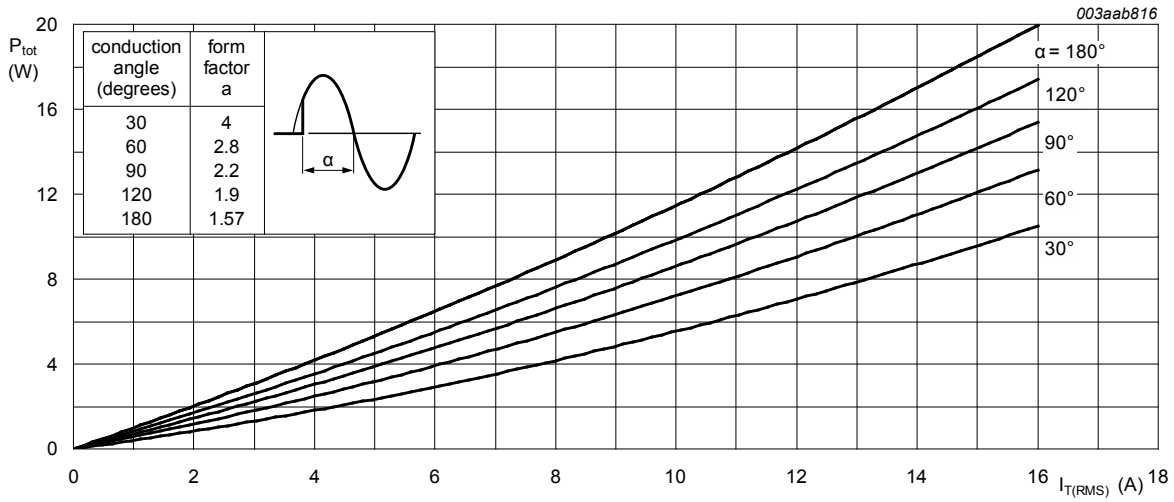


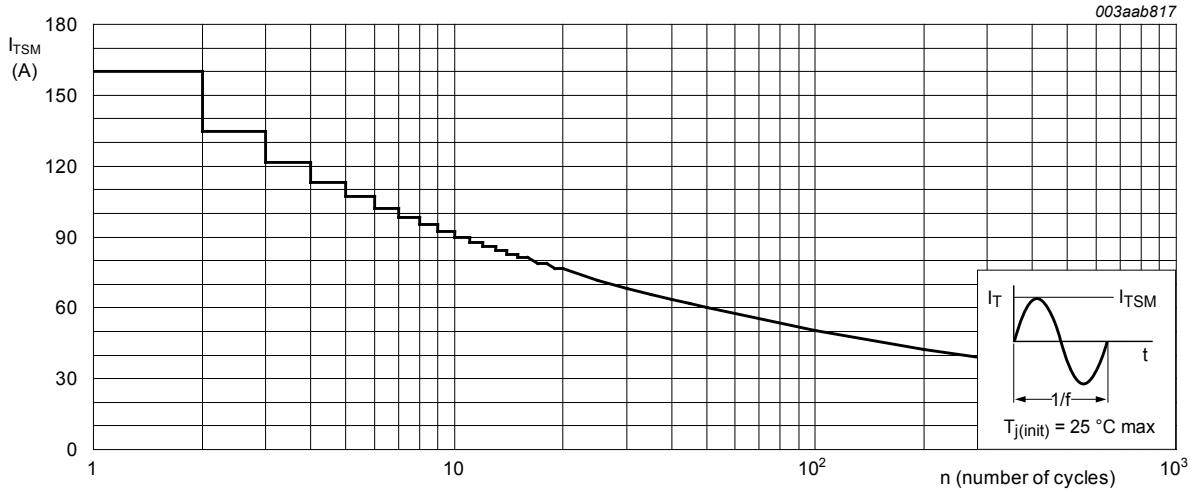
Fig. 2. RMS on-state current as a function of mounting base temperature; maximum values



α = conduction angle

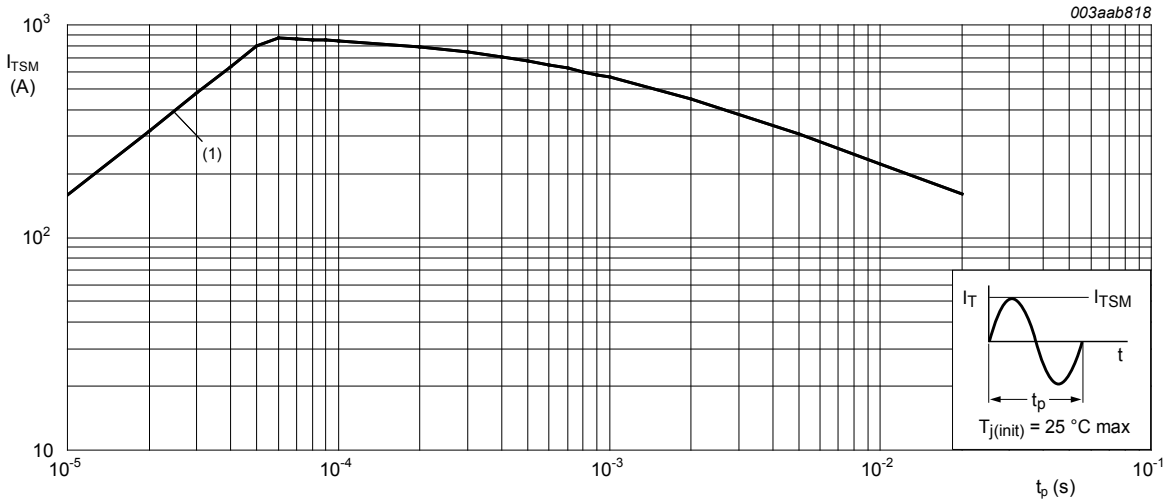
a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20$ ms

(1) dI_T/dt limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse duration; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	full cycle; Fig. 6		-	-	1.9	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		-	60	-	K/W

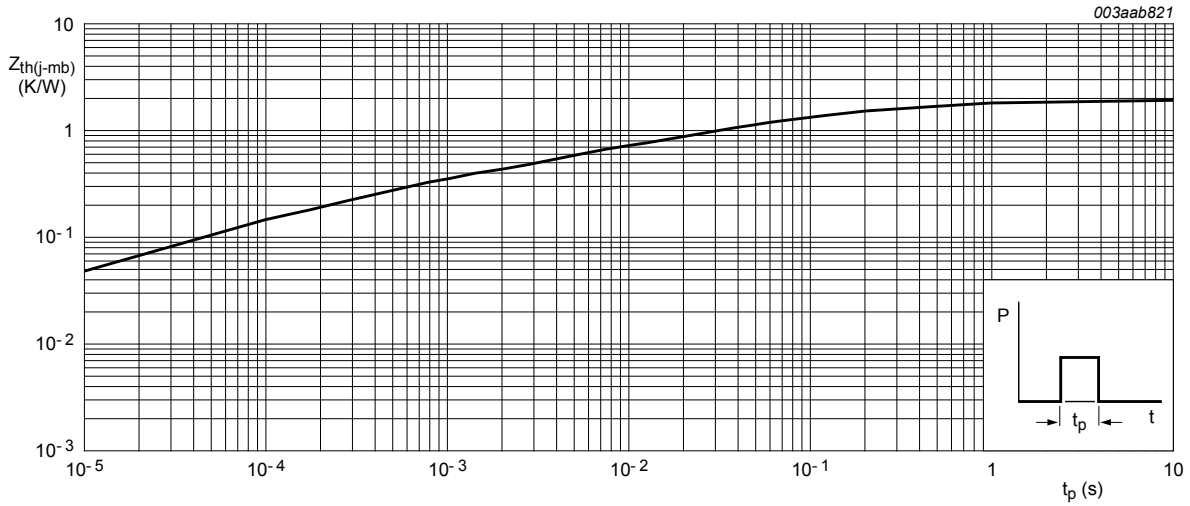


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse duration

9. Isolation characteristics

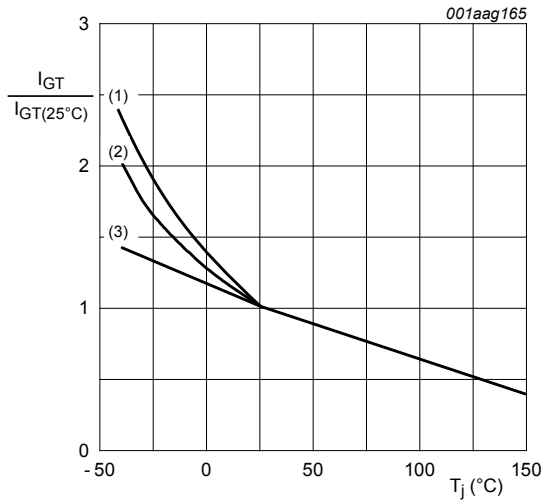
Table 6. Isolation characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; T_{mb} = 25 °C		-	-	2500	V
C_{isol}	isolation capacitance	from main terminal 2 to external heatsink; f = 1 MHz; T_{mb} = 25 °C		-	10	-	pF

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 7		2	-	50	mA
		V_D = 12 V; I_T = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 7		2	-	50	mA
		V_D = 12 V; I_T = 0.1 A; T2- G-; T_j = 25 °C; Fig. 7		2	-	50	mA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 8		-	-	60	mA
		V_D = 12 V; I_G = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 8		-	-	90	mA
		V_D = 12 V; I_G = 0.1 A; T2- G-; T_j = 25 °C; Fig. 8		-	-	60	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 9		-	-	60	mA
V_T	on-state voltage	I_T = 20 A; T_j = 25 °C; Fig. 10		-	1.2	1.5	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 11		-	0.7	1	V
		V_D = 400 V; I_T = 0.1 A; T_j = 150 °C		0.25	0.4	-	V
I_D	off-state current	V_D = 800 V; T_j = 125 °C		-	0.1	0.5	mA
		V_D = 800 V; T_j = 150 °C		-	0.4	2	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		1000	-	-	V/µs
		V_{DM} = 536 V; T_j = 150 °C; (V_{DM} = 67% of V_{DRM}); exponential waveeform; gate open circuit		600	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 16 A; dV_{com}/dt = 20 V/µs; (without snubber condition); gate open circuit		15	-	-	A/ms
		V_D = 400 V; T_j = 150 °C; $I_{T(RMS)}$ = 16 A; dV_{com}/dt = 20 V/µs; (without snubber condition); gate open circuit		6	-	-	A/ms



(1) T2- G-
(2) T2+ G-
(3) T2+ G+

Fig. 7. Normalized gate trigger current as a function of junction temperature

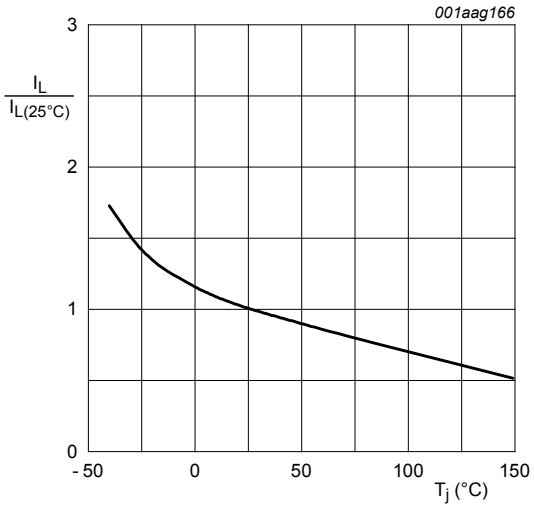


Fig. 8. Normalized latching current as a function of junction temperature

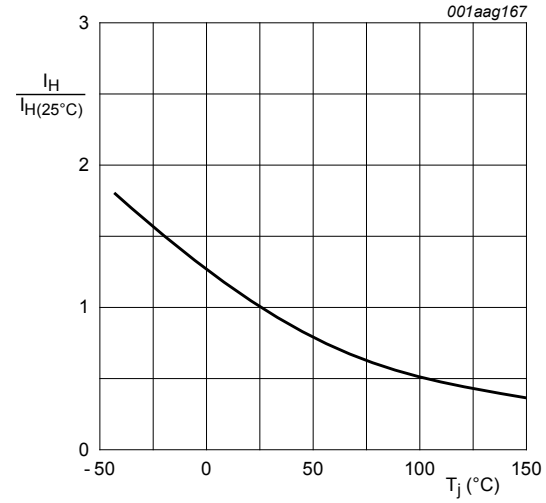
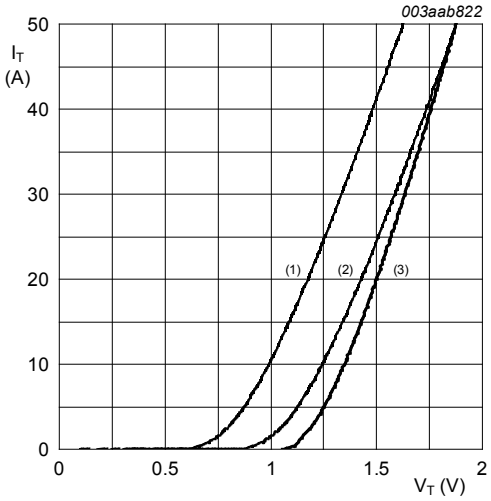


Fig. 9. Normalized holding current as a function of junction temperature



V_o = 1.086 V; R_s = 0.017 Ω
(1) T_j = 150 °C; typical values
(2) T_j = 150 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

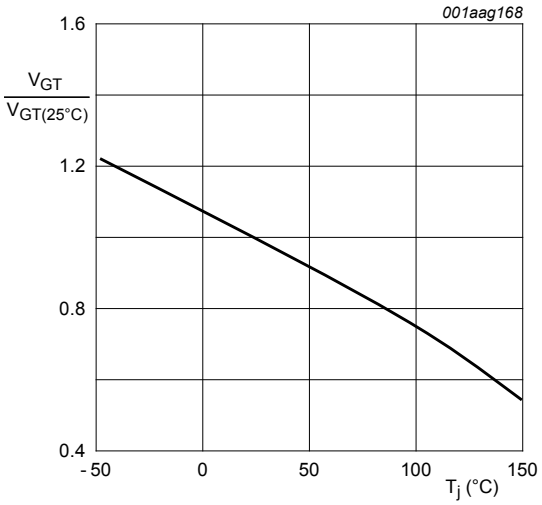
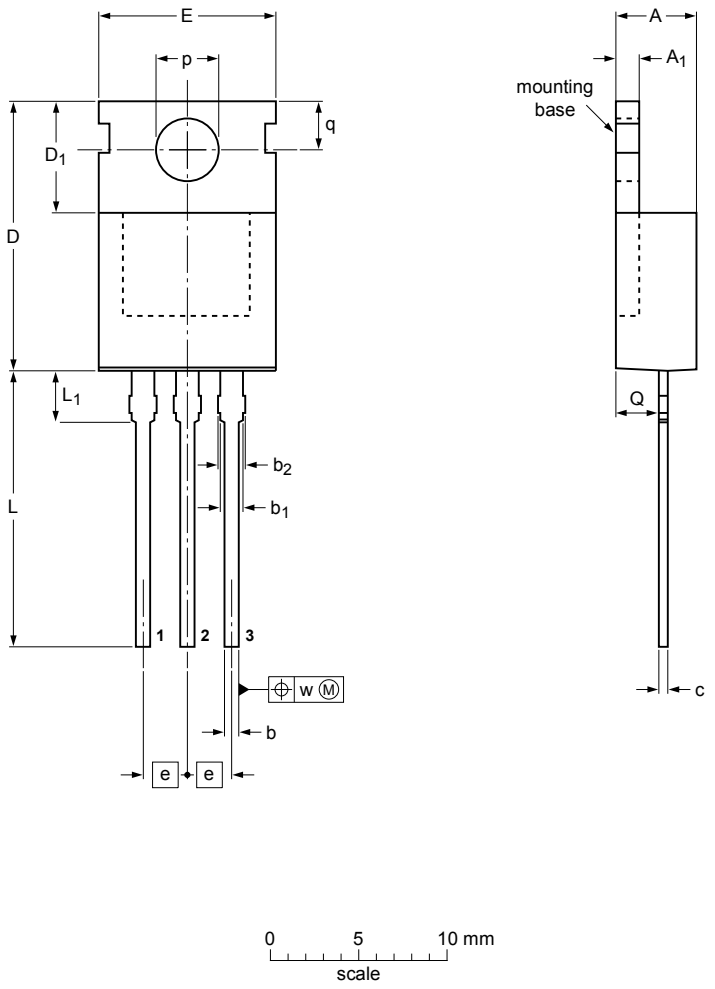


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

11. Package outline

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 **SOT78D**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D	D_1 ref	E	e	L	L_1 ref	p	Q	q	w
mm	4.7 4.3	1.40 1.25	0.9 0.6	1.4 1.1	1.72 1.32	0.6 0.4	16.0 15.2	6.5	10.3 9.7	2.54	14.0 12.8	3.0	3.7 3.5	2.6 2.2	3.0 2.7	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT78D		TO-220				~~07-04-04~~ 07-07-10

Fig. 12. Package outline TO-220AB (SOT78D)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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