
# BUK9614-60E

## N-channel TrenchMOS logic level FET

**28 July 2016** **Product data sheet**

## 1. General description

Logic level N-channel MOSFET in a SOT404 package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

## 2. Features and benefits

- AEC Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with VGS(th) rating of greater than 0.5V at 175 °C

## 3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

## 4. Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j \geq 25$ °C; $T_j \leq 175$ °C | | - | - | 60 | V |
| $I_D$ | drain current | $V_{GS}$ = 5 V; $T_{mb}$ = 25 °C; Fig. 2 | | - | - | 56 | A |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | - | 96 | W |
| **Static characteristics** | | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 5 V; $I_D$ = 15 A; $T_j$ = 25 °C; Fig. 11 | | - | 11.5 | 14 | mΩ |
| **Dynamic characteristics** | | | | | | | |
| $Q_{GD}$ | gate-drain charge | $V_{GS}$ = 5 V; $I_D$ = 15 A; $V_{DS}$ = 48 V; Fig. 13; Fig. 14 | | - | 6.7 | - | nC |

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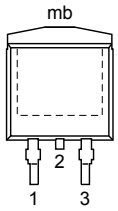
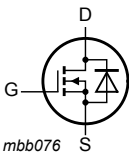
## 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | G | gate |   D2PAK (SOT404) |   |
| 2 | D | drain | | |
| 3 | S | source | | |
| mb | D | mounting base; connected to drain | | |

## 6. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| BUK9614-60E | D2PAK | plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) | SOT404 |

## 7. Marking

**Table 4. Marking codes**

| Type number | Marking code |
|---|---|
| BUK9614-60E | BUK9614-60E |

## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j \geq 25$ °C; $T_j \leq 175$ °C | | - | 60 | V |
| $V_{DGR}$ | drain-gate voltage | $R_{GS}$ = 20 kΩ | | - | 60 | V |
| $V_{GS}$ | gate-source voltage | $T_j \leq 175$ °C; DC | | -10 | 10 | V |
| | | $T_j \leq 175$ °C; Pulsed | [1][2] | -15 | 15 | V |
| $P_{tot}$ | total power dissipation | $T_{mb}$ = 25 °C; Fig. 1 | | - | 96 | W |
| $I_D$ | drain current | $T_{mb}$ = 25 °C; $V_{GS}$ = 5 V; Fig. 2 | | - | 56 | A |
| | | $T_{mb}$ = 100 °C; $V_{GS}$ = 5 V; Fig. 2 | | - | 40 | A |
| $I_{DM}$ | peak drain current | $T_{mb}$ = 25 °C; pulsed; $t_p \leq 10$ µs; Fig. 3 | | - | 224 | A |
| $T_{stg}$ | storage temperature | | | -55 | 175 | °C |

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $T_j$ | junction temperature | | | -55 | 175 | °C |
| **Source-drain diode** | | | | | | |
| $I_S$ | source current | $T_{mb}$ = 25 °C | [3] | - | 56 | A |
| $I_{SM}$ | peak source current | pulsed; $t_p \leq 10$ µs; $T_{mb}$ = 25 °C | | - | 224 | A |
| **Avalanche ruggedness** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $I_D$ = 56 A; $V_{sup} \leq 60$ V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4 | [4][5] | - | 39 | mJ |

[1] Accumulated pulse duration up to 50 hours delivers zero defect ppm
[2] Significantly longer life times are achieved by lowering $T_j$ and or $V_{GS}$
[3] Continuous current is limited by package.
[4] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[5] Refer to application note AN10273 for further information.

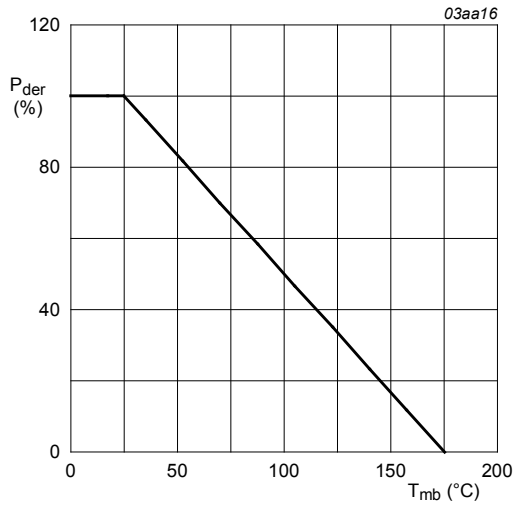



**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

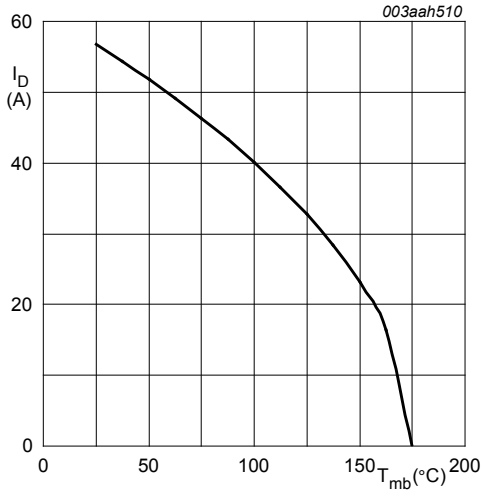



**Fig. 2. Continuous drain current as a function of mounting base temperature**

$V_{GS} \geq 5V$

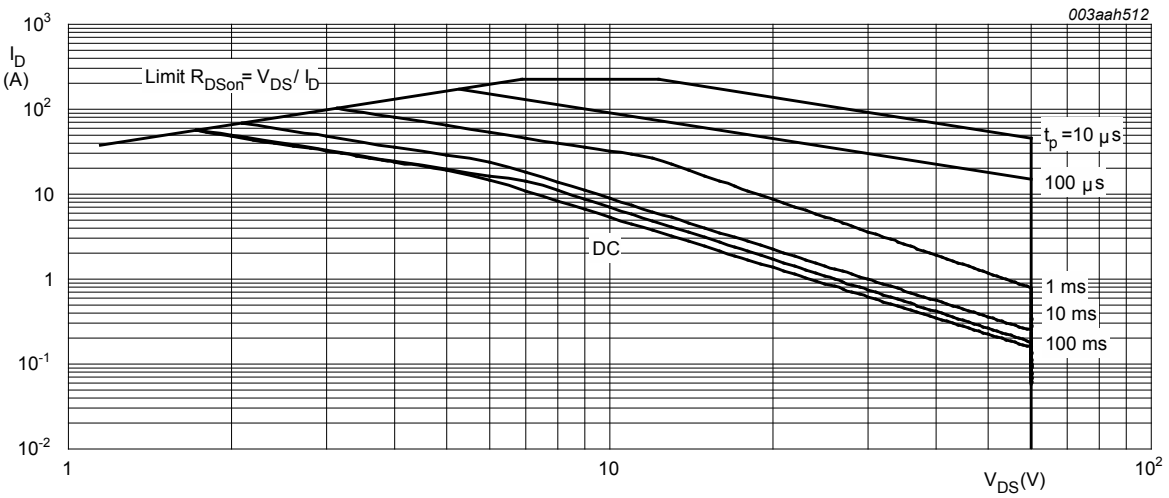



**Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

$T_{mb} = 25°C$; $I_{DM}$ *is a single pulse*

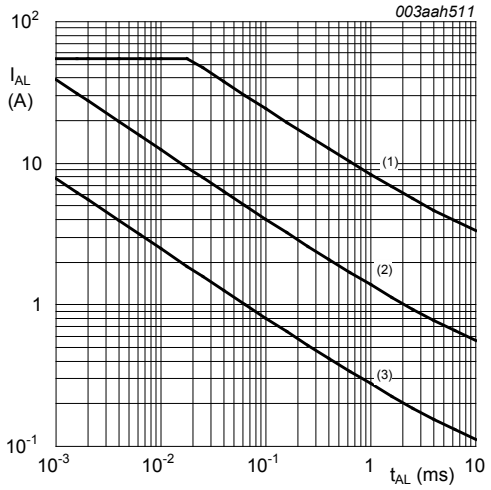



**Fig. 4. Single pulse avalanche rating; avalanche current as a function of avalanche time**

(1) $T_{j(init)} = 25°C$; (2) $T_{j(init)} = 150°C$; (3) Repetitive Avalanche

# 9. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | Fig. 5 | | - | - | 1.56 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | minimum footprint ; mounted on a printed-circuit board | | - | 50 | - | K/W |

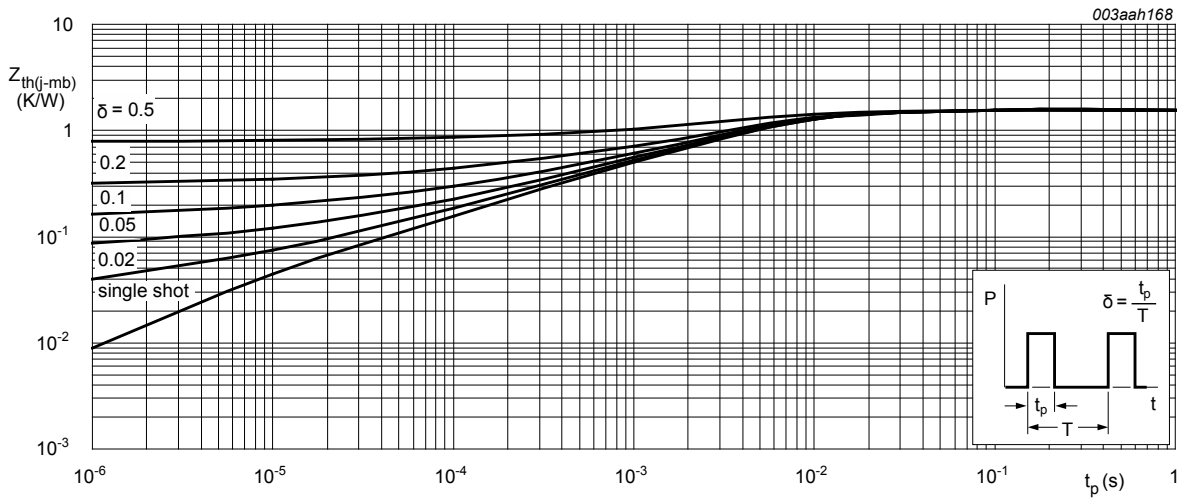


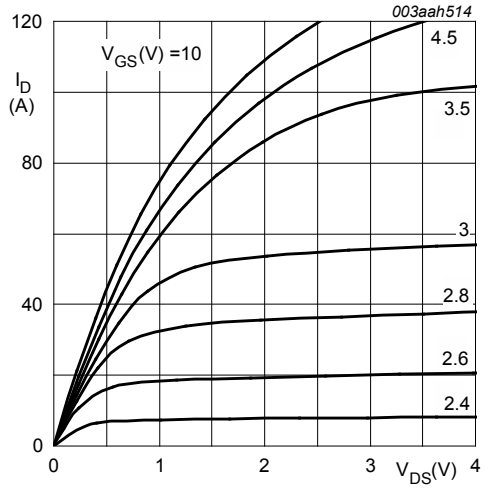

**Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration**

## 10. Characteristics

**Table 7. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | 60 | - | - | V |
| | | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = -55 °C | | 54 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 25 °C; Fig. 9; Fig. 10 | | 1.4 | 1.7 | 2.1 | V |
| | | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = -55 °C; Fig. 9 | | - | - | 2.45 | V |
| | | $I_D$ = 1 mA; $V_{DS}$ = $V_{GS}$; $T_j$ = 175 °C; Fig. 9 | | 0.5 | - | - | V |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 60 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | - | 0.02 | 1 | µA |
| | | $V_{DS}$ = 60 V; $V_{GS}$ = 0 V; $T_j$ = 175 °C | | - | - | 500 | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 10 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | 2 | 100 | nA |
| | | $V_{GS}$ = -10 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | 2 | 100 | nA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 5 V; $I_D$ = 15 A; $T_j$ = 25 °C; Fig. 11 | | - | 11.5 | 14 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 15 A; $T_j$ = 25 °C; Fig. 11 | | - | 10.3 | 12.8 | mΩ |
| | | $V_{GS}$ = 5 V; $I_D$ = 15 A; $T_j$ = 175 °C; Fig. 12; Fig. 11 | | - | - | 31 | mΩ |
| **Dynamic characteristics** | | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D$ = 15 A; $V_{DS}$ = 48 V; $V_{GS}$ = 5 V; Fig. 13; Fig. 14 | | - | 20.5 | - | nC |
| $Q_{GS}$ | gate-source charge | | | - | 4 | - | nC |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $Q_{GD}$ | gate-drain charge | | | - | 6.7 | - | nC |
| $C_{iss}$ | input capacitance | $V_{GS}$ = 0 V; $V_{DS}$ = 25 V; f = 1 MHz; $T_j$ = 25 °C; Fig. 15 | | - | 1988 | 2651 | pF |
| $C_{oss}$ | output capacitance | | | - | 196 | 235 | pF |
| $C_{rss}$ | reverse transfer capacitance | | | - | 114 | 156 | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 45 V; $R_L$ = 3 Ω; $V_{GS}$ = 5 V; $R_{G(ext)}$ = 5 Ω | | - | 16.9 | - | ns |
| $t_r$ | rise time | | | - | 22.4 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | | - | 35.7 | - | ns |
| $t_f$ | fall time | | | - | 22.9 | - | ns |
| $L_D$ | internal drain inductance | from upper edge of drain mounting base to center of die | | - | 2.5 | - | nH |
| $L_S$ | internal source inductance | from source lead to source bonding pad | | - | 7.5 | - | nH |
| **Source-drain diode** | | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 15 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C; Fig. 16 | | - | 0.83 | 1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 15 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 25 V | | - | 22.3 | - | ns |
| $Q_r$ | recovered charge | | | - | 20.9 | - | nC |




$T_j$ = 25 °C; $t_p$ = 300 µs

**Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values**

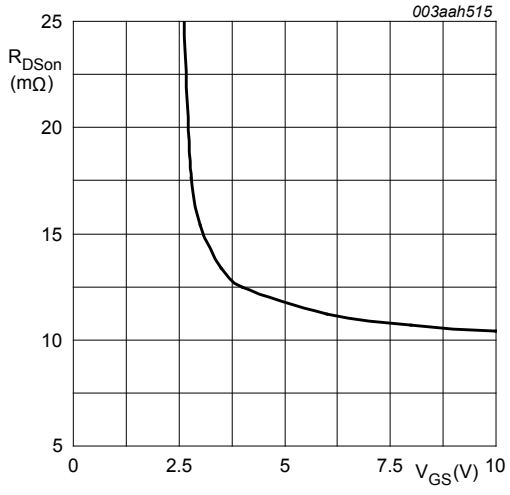



**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values**

$T_j = 25°C;\ I_D = 15A$

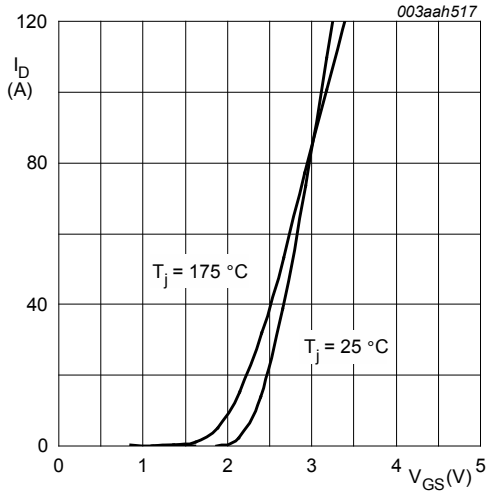



**Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values**

$V_{DS} = 10V$

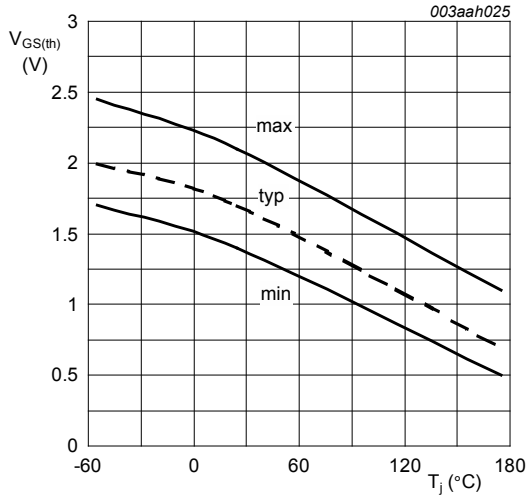



**Fig. 9. Gate-source threshold voltage as a function of junction temperature**

$I_D = 1$ mA; $V_{DS} = V_{GS}$

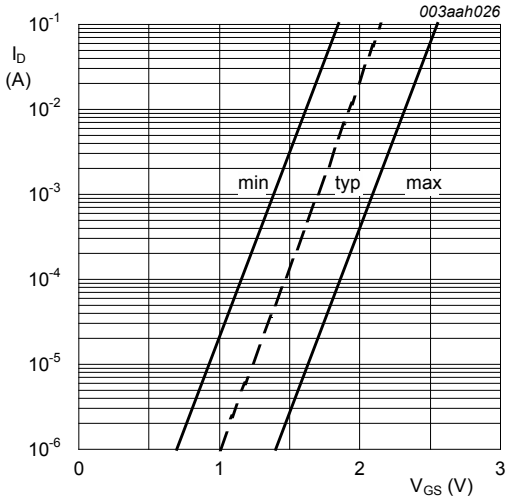
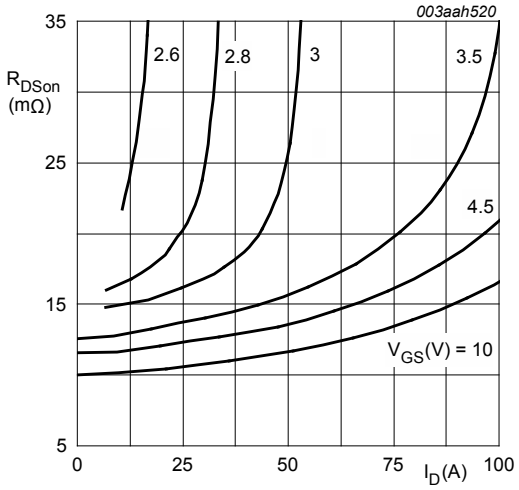



**Fig. 10. Sub-threshold drain current as a function of gate-source voltage**

$T_j = 25°C$; $V_{DS} = 5V$




$T_j$ = 25 °C; $t_p$ = 300 µs

**Fig. 11. Drain-source on-state resistance as a function of drain current; typical values**

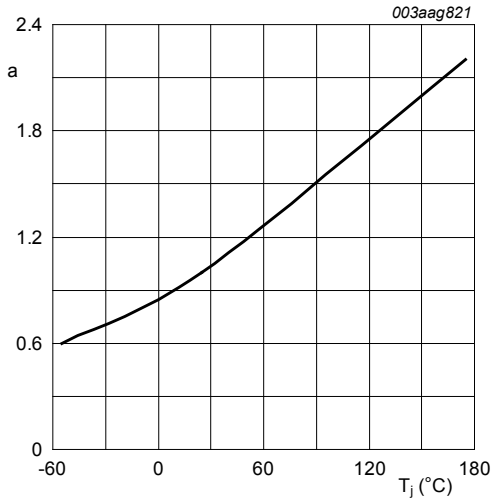



**Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature**

$$a = \frac{R_{DSon}}{R_{DSon(25\,°C)}}$$

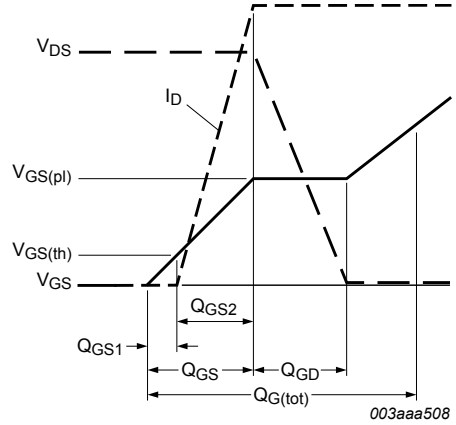



**Fig. 13. Gate charge waveform definitions**

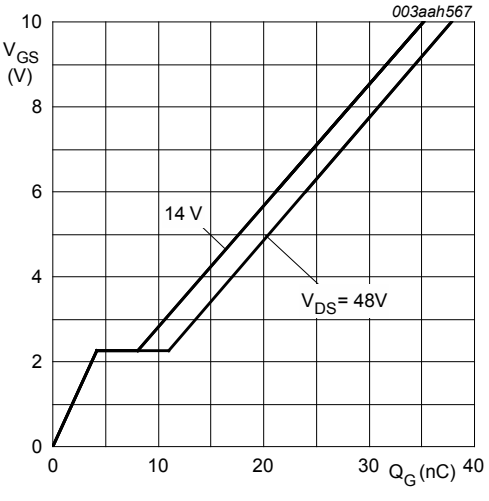



**Fig. 14. Gate-source voltage as a function of gate charge; typical values**

$$T_j = 25°C;\ I_D = 15A$$

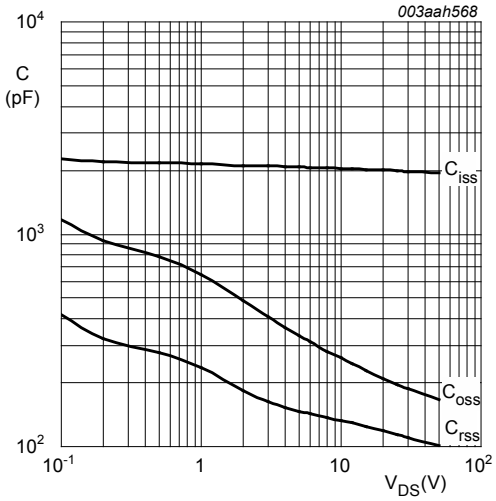



**Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

$$V_{GS} = 0V;\ f = 1MHz$$

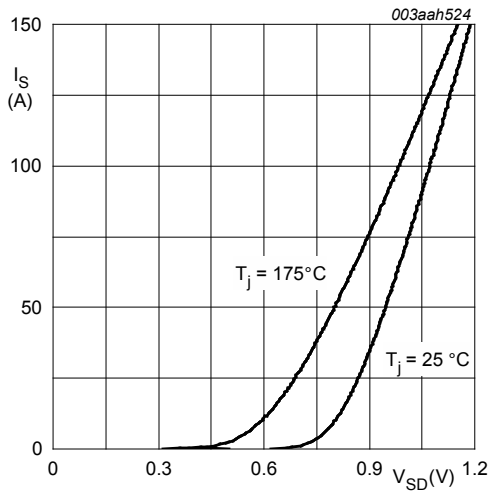
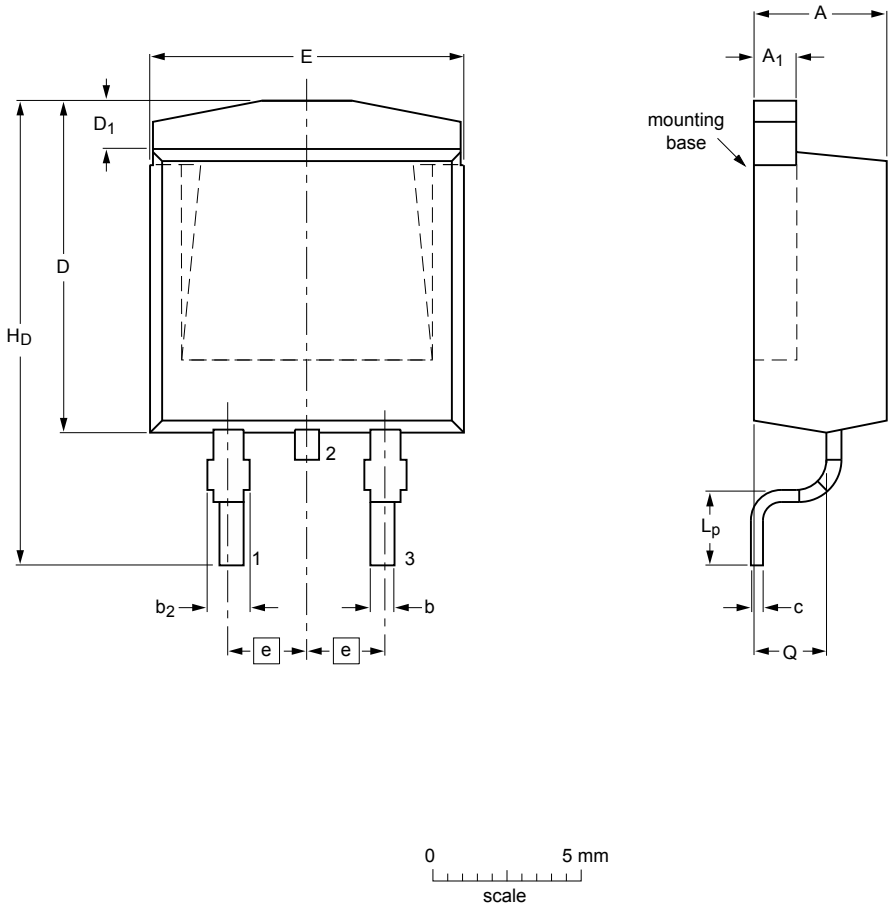



**Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values**

$V_{GS} = 0V$

# 11. Package outline

**Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)** **SOT404**




Dimensions (mm are the original dimensions)

| Unit | | A | $A_1$ | b | $b_2$ | c | D | $D_1$ | E | e | $H_D$ | $L_p$ | Q |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 4.5 | 1.40 | 0.85 | 1.45 | 0.64 | 11 | 1.6 | 10.3 | | 15.8 | 2.9 | 2.6 |
| | nom | | | | | | | | | 2.54 | | | |
| | min | 4.1 | 1.27 | 0.60 | 1.05 | 0.46 | | 1.2 | 9.7 | | 14.8 | 2.1 | 2.2 |

*sot404_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT404 | | | | | | ~~06-03-16~~ 13-02-25 |

**Fig. 17. Package outline D2PAK (SOT404)**

# 12. Legal information

## 12.1 Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
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[1] Please consult the most recently issued document before initiating or completing a design.
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