



BUK9K18-40E

Dual N-channel 40 V, 19.5 mΩ logic level MOSFET

16 March 2016

Product data sheet

1. General description

Dual logic level N-channel MOSFET in an LPAK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Dual MOSFET
- Q101 Compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with $V_{GS(th)}$ rating of greater than 0.5 V at 175 °C

3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	40	V
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	30	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	38	W
Static characteristics FET1 and FET2						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 10\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12	-	17.1	19.5	mΩ
Dynamic characteristics FET1 and FET2						
Q_{GD}	gate-drain charge	$I_D = 10\text{ A}$; $V_{DS} = 32\text{ V}$; $V_{GS} = 10\text{ V}$; $T_j = 25\text{ °C}$; Fig. 14	-	3	-	nC

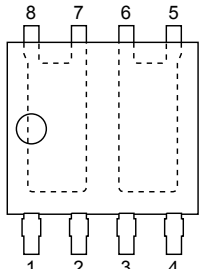
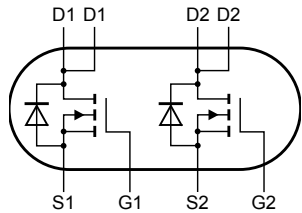


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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>LFPAK56D (SOT1205)</p>	 <p><i>mbk725</i></p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9K18-40E	LFPAK56D	Plastic single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9K18-40E	91840E

8. Limiting values

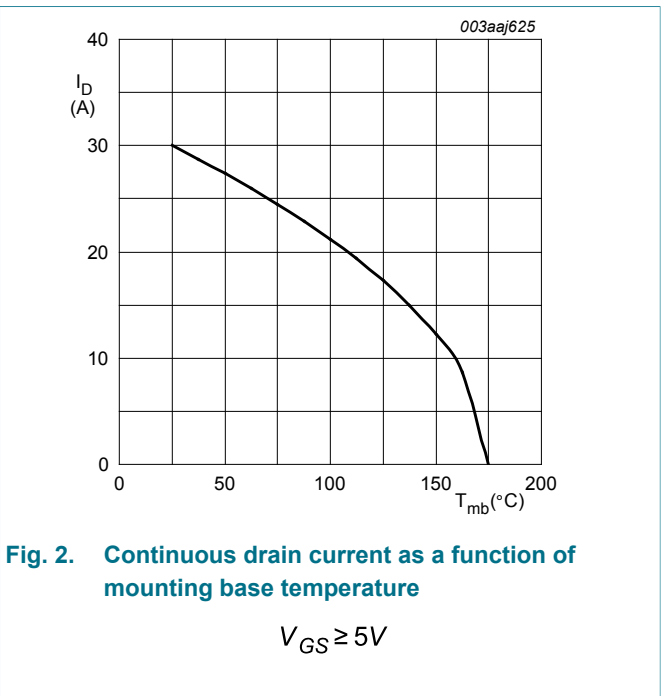
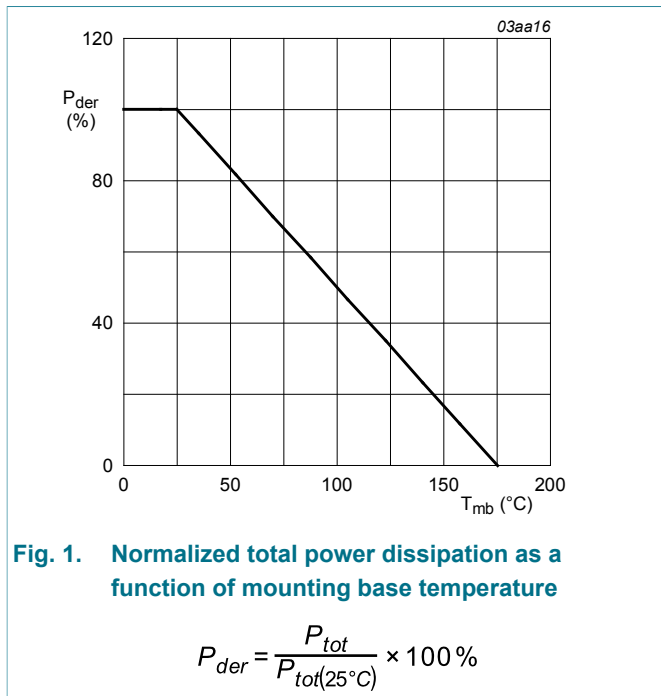
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	40	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	40	V
V_{GS}	gate-source voltage	DC; $T_j \leq 175\text{ °C}$	-10	10	V
		Pulsed; $T_j \leq 175\text{ °C}$	[1][2]	15	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	38	W
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	30	A
		$V_{GS} = 5\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2	-	24	A

Symbol	Parameter	Conditions	Min	Max	Unit
I_{DM}	peak drain current	pulsed; $t_p \leq 10 \mu s$; $T_{mb} = 25 \text{ }^\circ\text{C}$; Fig. 3	-	124	A
T_{stg}	storage temperature		-55	175	$^\circ\text{C}$
T_j	junction temperature		-55	175	$^\circ\text{C}$
$T_{sl(M)}$	peak soldering temperature		-	260	$^\circ\text{C}$
Source-drain diode FET1 and FET2					
I_S	source current	$T_{mb} = 25 \text{ }^\circ\text{C}$	-	30	A
I_{SM}	peak source current	pulsed; $t_p \leq 10 \mu s$; $T_{mb} = 25 \text{ }^\circ\text{C}$	-	124	A
Avalanche Ruggedness FET1 and FET2					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 30 \text{ A}$; $V_{sup} \leq 40 \text{ V}$; $V_{GS} = 5 \text{ V}$; $T_{j(\text{init})} = 25 \text{ }^\circ\text{C}$; Fig. 4	[3][4]	-	22 mJ

- [1] Accumulated Pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T_j and or V_{GS} .
- [3] Refer to application note AN10273 for further information
- [4] Single-pulse avalanche rating limited by maximum junction temperature of 175 $^\circ\text{C}$



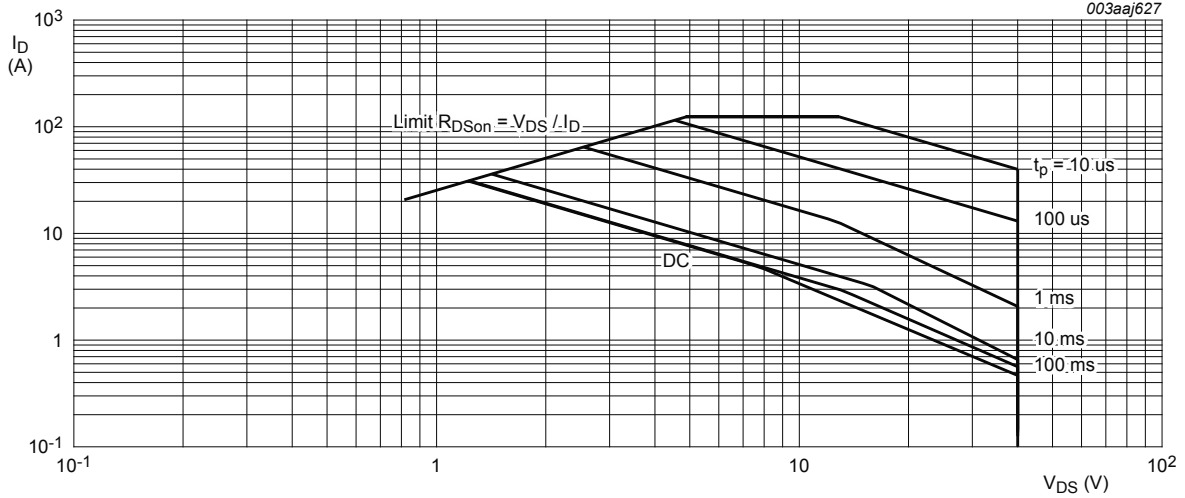


Fig. 3. Safe operating area; continuous and peak drain current as a function of drain-source voltage

$T_{mb} = 25^\circ C; I_{DM}$ is single pulse

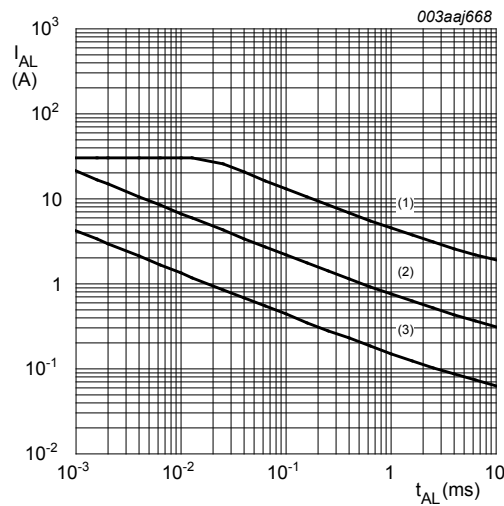


Fig. 4. Single-pulse and repetitive avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2

- (1) Single-pulse; $T_j = 25^\circ C$.
- (2) Single-pulse; $T_j = 150^\circ C$.
- (3) Repetitive.

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	3.96	K/W

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

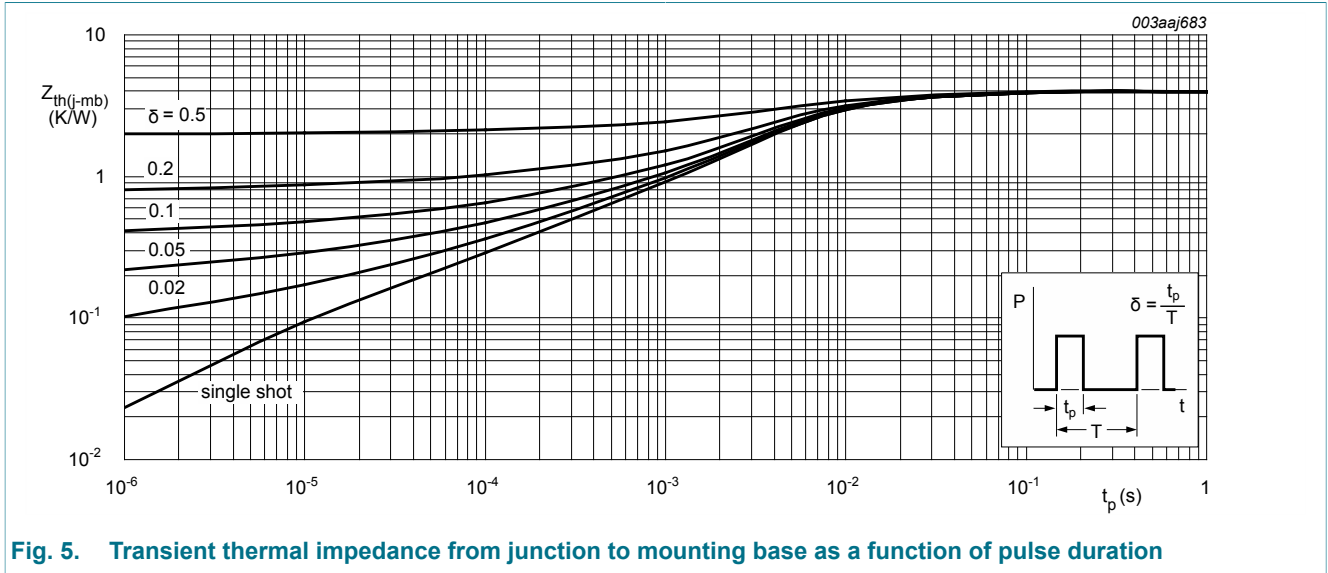


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics FET1 and FET2						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C;$ Fig. 10; Fig. 11	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C;$ Fig. 10; Fig. 11	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C;$ Fig. 10; Fig. 11	-	-	2.45	V
I_{DSS}	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	-	500	μA
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.02	1	μA
I_{GSS}	gate leakage current	$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ }^\circ C;$ Fig. 12	-	17.1	19.5	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 10 \text{ A}; T_j = 175 \text{ }^\circ C;$ Fig. 12; Fig. 13	-	34.37	39.2	mΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_{GS} = 10\text{ V}; I_D = 10\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 12	-	13.5	16	mΩ
Dynamic characteristics FET1 and FET2						
$Q_{G(\text{tot})}$	total gate charge	$I_D = 10\text{ A}; V_{DS} = 32\text{ V}; V_{GS} = 10\text{ V};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 14 ; Fig. 15	-	14.5	-	nC
Q_{GS}	gate-source charge	$I_D = 10\text{ A}; V_{DS} = 32\text{ V}; V_{GS} = 10\text{ V};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 14	-	2	-	nC
Q_{GD}	gate-drain charge		-	3	-	nC
C_{iss}	input capacitance	$V_{DS} = 25\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^\circ\text{C};$ Fig. 16	-	796	1061	pF
C_{oss}	output capacitance		-	137	164	pF
C_{rss}	reverse transfer capacitance		-	82	112	pF
$t_{d(\text{on})}$	turn-on delay time	$V_{DS} = 32\text{ V}; R_L = 3.3\text{ }^\Omega; V_{GS} = 10\text{ V};$ $R_{G(\text{ext})} = 5\text{ }^\Omega; T_j = 25\text{ }^\circ\text{C}$	-	4	-	ns
t_r	rise time		-	4.6	-	ns
$t_{d(\text{off})}$	turn-off delay time		-	17.5	-	ns
t_f	fall time		-	9.9	-	ns
Source-drain diode FET1 and FET2						
V_{SD}	source-drain voltage	$I_S = 10\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 17	-	0.78	1.2	V
t_{rr}	reverse recovery time	$I_S = 10\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 20\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	8.3	-	ns
Q_r	recovered charge		-	16.2	-	nC

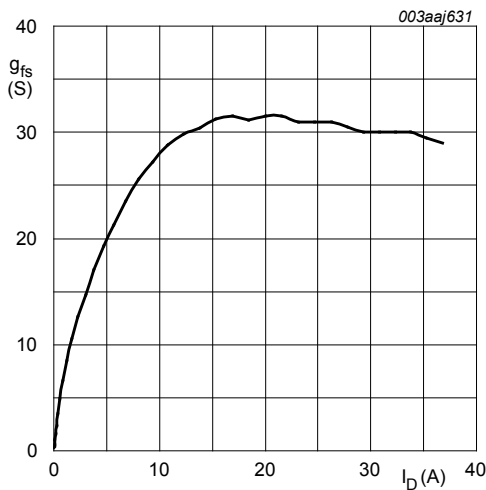


Fig. 6. Forward transconductance as a function of drain current; typical values

$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 5\text{ V}$

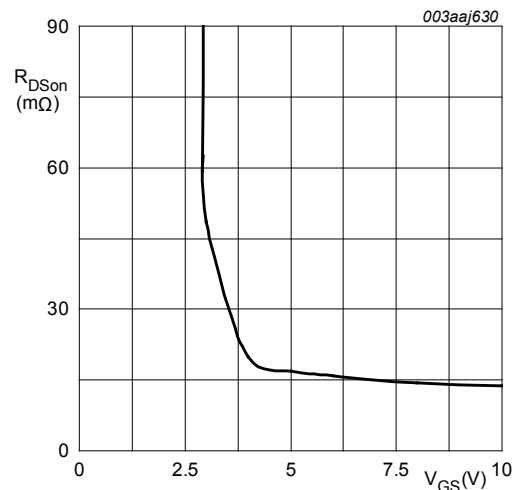
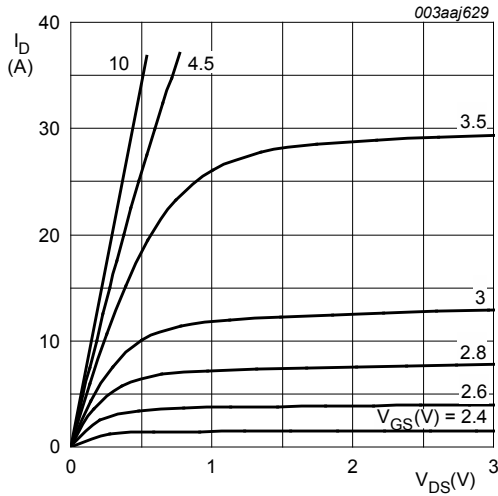


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25\text{ }^\circ\text{C}; I_D = 10\text{ A}$



$T_j = 25\text{ }^\circ\text{C}; t_p = 300\text{ }\mu\text{s}$

Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

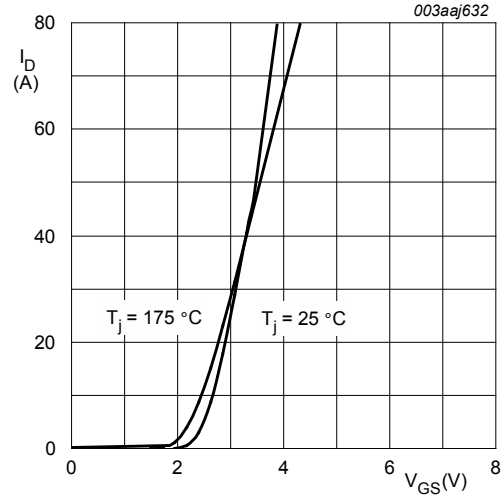


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10\text{ V}$

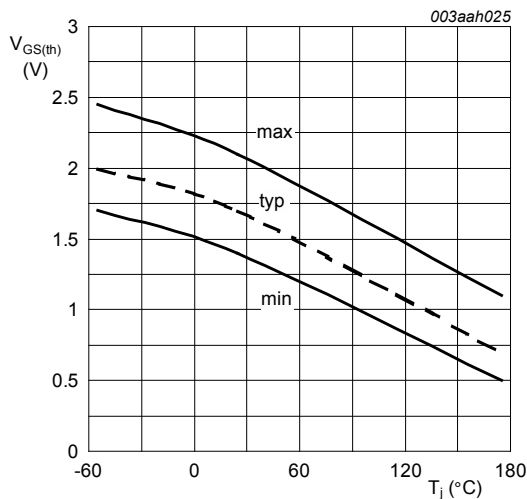


Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

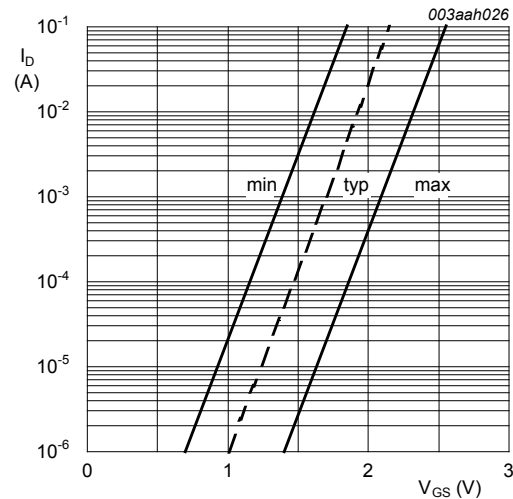
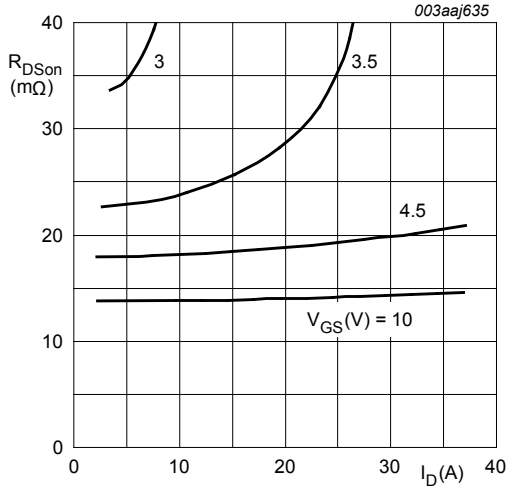


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 5\text{ V}$



$T_j = 25^\circ\text{C}; t_p = 300 \mu\text{s}$

Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

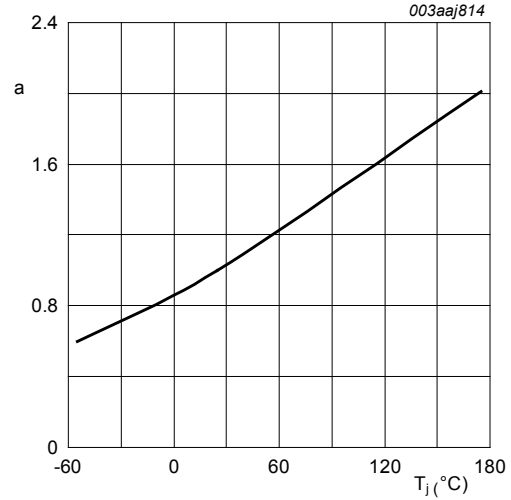


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DS(on)}}{R_{DS(on)}(25^\circ\text{C})}$$

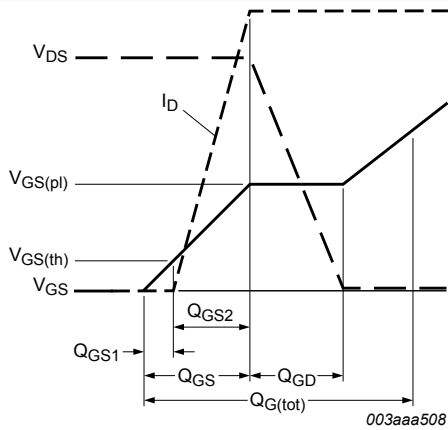


Fig. 14. Gate charge waveform definitions

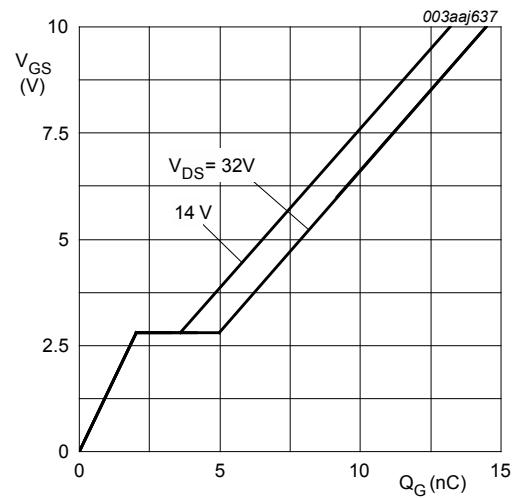


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ\text{C}; I_D = 10\text{A}$

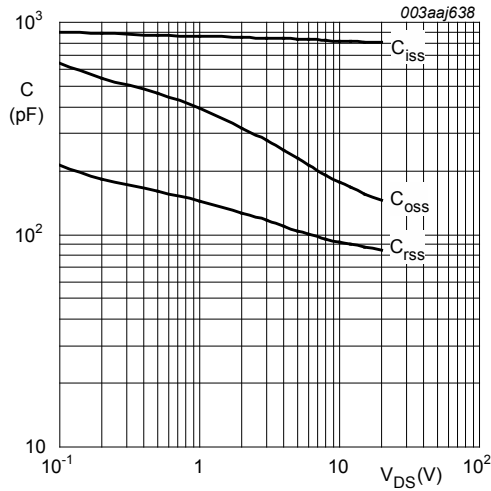


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0V; f = 1MHz$$

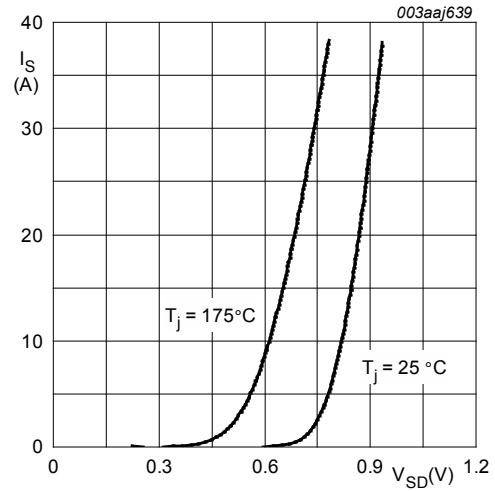


Fig. 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

11. Package outline

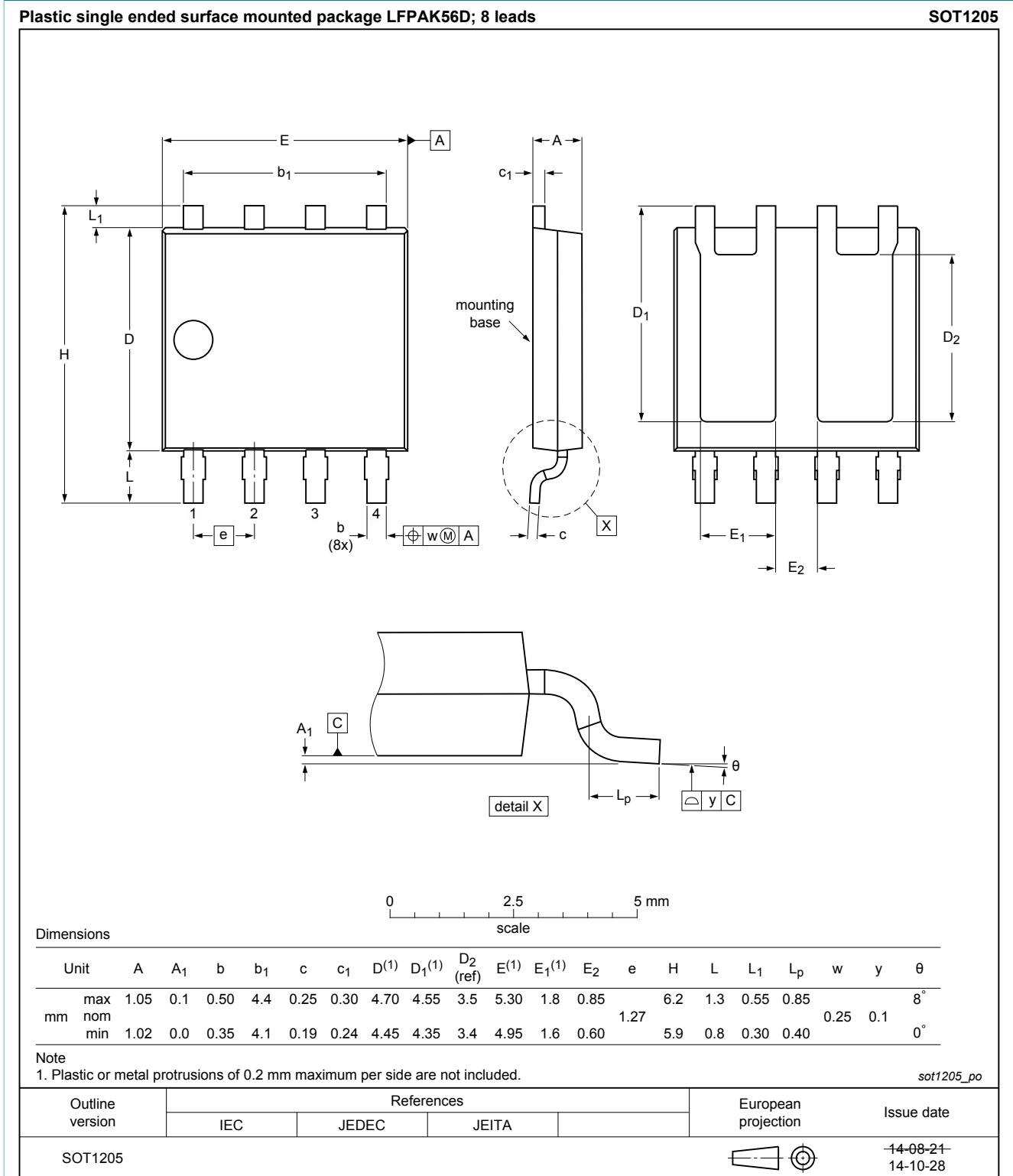


Fig. 18. Package outline LFPAK56D (SOT1205)

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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