DATA SHEET

PEMB3; PUMB3
PNP/PNP resistor-equipped transistors; R1 = 4.7 kΩ, R2 = open

Product data sheet

Supersedes data of 2001 Sep 19

2003 Oct 15

NXP

founded by Philips

PNP/PNP resistor-equipped transistors; R1 = 4.7 kΩ, R2 = open

PEMB3; PUMB3

FEATURES

- Built-in bias resistors
- Simplified circuit design
- Reduction of component count
- Reduced pick and place costs.

APPLICATIONS

- Low current peripheral drivers
- Replacement of general purpose transistors in digital applications
- Control of IC inputs.

DESCRIPTION

PNP/PNP resistor-equipped transistors (see "Simplified outline, symbol and pinning" for package details).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
V_{CEO}	collector-emitter voltage	–	−50	V
I_O	output current (DC)	–	−100	mA
TR1	PNP	–	–	–
TR2	PNP	–	–	–
R1	bias resistor	4.7	–	kΩ
R2	bias resistor	open	–	–

PRODUCT OVERVIEW

TYPE NUMBER	PACKAGE		MARKING CODE	NPN/PNP COMPLEMENT	NPN/NPN COMPLEMENT
	PHILIPS	EIAJ			
PEMB3	SOT666	–	Z3	PEMD6	PEMH7
PUMB3	SOT363	SC-88	B5*[1]	PUMD6	PUMH7

Note

1. * = p: Made in Hong Kong.
   * = t: Made in Malaysia.
   * = W: Made in China.

SIMPLIFIED OUTLINE, SYMBOL AND PINNING

TYPE NUMBER	SIMPLIFIED OUTLINE AND SYMBOL	PINNING	
		PIN	DESCRIPTION
PEMB3 PUMB3	Top view MAM452	1	emitter TR1
		2	base TR1
		3	collector TR2
		4	emitter TR2
		5	base TR2
		6	collector TR1

PNP/PNP resistor-equipped transistors; R1 = 4.7 kΩ, R2 = open	PEMB3; PUMB3

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PEMB3	–	plastic surface mounted package; 6 leads	SOT666
PUMB3	–	plastic surface mounted package; 6 leads	SOT363

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor					
V_{CBO}	collector-base voltage	open emitter	–	−50	V
V_{CEO}	collector-emitter voltage	open base	–	−50	V
V_{EBO}	emitter-base voltage	open collector	–	−5	V
I_O	output current (DC)		–	−100	mA
I_{CM}	peak collector current		–	−100	mA

P_{tot}	total power dissipation
	    SOT363
	    SOT666
		$T_{amb} \leq 25$ °C
		note 1
		notes 1 and 2
			–
			–
				200
				200
					mW
					mW

T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		–	150	°C
T_{amb}	operating ambient temperature		−65	+150	°C
Per device					

P_{tot}	total power dissipation
	    SOT363
	    SOT666
		$T_{amb} \leq 25$ °C
		note 1
		notes 1 and 2
			–
			–
				300
				300
					mW
					mW

Notes

1. Device mounted on an FR4 printed-circuit board, single-sided copper, standard footprint.

2. Reflow soldering is the only recommended soldering method.

PNP/PNP resistor-equipped transistors;
R1 = 4.7 kΩ, R2 = open

PEMB3; PUMB3

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
Per transistor				
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	$T_{amb} \leq 25\ °C$		
	SOT363	note 1	625	K/W
	SOT666	notes 1 and 2	625	K/W
Per device				
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient	$T_{amb} \leq 25\ °C$		
	SOT363	note 1	416	K/W
	SOT666	note 1	416	K/W

Notes

1. Device mounted on an FR4 printed-circuit board, single-sided copper, standard footprint.

2. Reflow soldering is the only recommended soldering method.

CHARACTERISTICS

$T_{amb} = 25\ °C$ unless otherwise specified.

| SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	$V_{CB} = -50\ V$; $I_E = 0$	–	–	–100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = -30\ V$; $I_B = 0$	–	–	–1	μA
		$V_{CE} = -30\ V$; $I_B = 0$; $T_j = 150\ °C$	–	–	–50	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = -5\ V$; $I_C = 0$	–	–	–100	nA
h_{FE}	DC current gain	$V_{CE} = -5\ V$; $I_C = -1\ mA$	200	–	–	
V_{CEsat}	saturation voltage	$I_C = -5\ mA$; $I_B = -0.25\ mA$	–	–	–100	mV
R1	input resistor		3.3	4.7	6.1	kΩ
C_c	collector capacitance	$I_E = i_e = 0$; $V_{CB} = -10\ V$; $f = 1\ MHz$	–	–	3	pF

PNP/PNP resistor-equipped transistors;
R1 = 4.7 kΩ, R2 = open

PEMB3; PUMB3

PACKAGE OUTLINES

Plastic surface mounted package; 6 leads

SOT666

detail X

scale
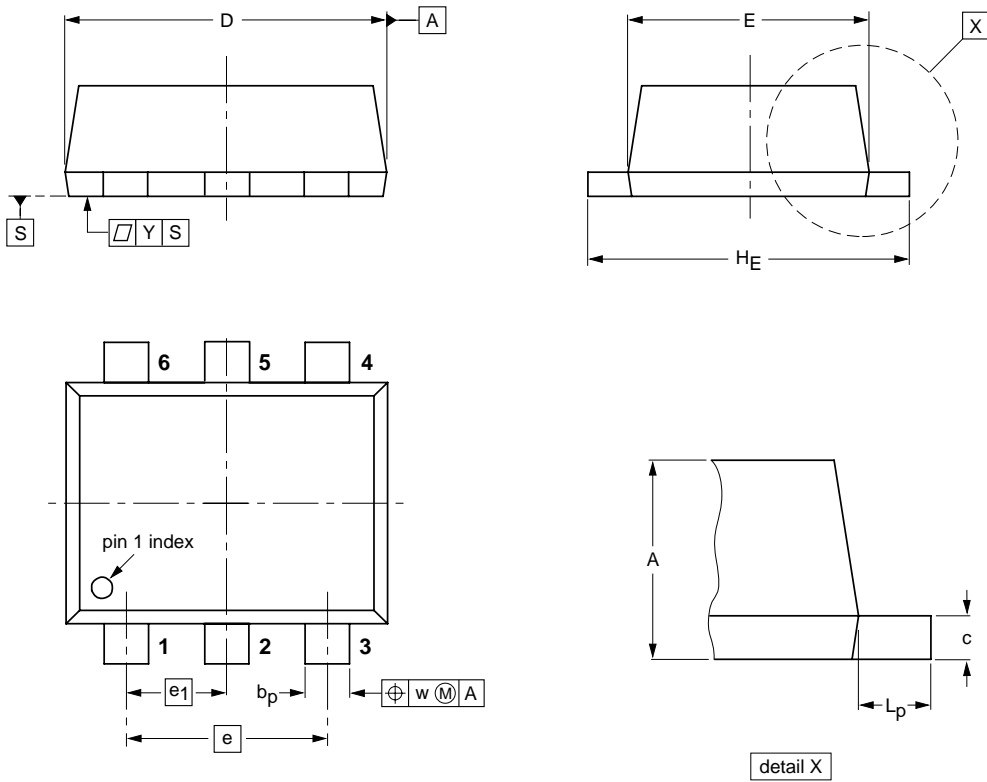
DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	e	e_1	H_E	L_p	w	y
mm	0.6 0.5	0.27 0.17	0.18 0.08	1.7 1.5	1.3 1.1	1.0	0.5	1.7 1.5	0.3 0.1	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT666						~~01-01-04~~ 01-08-27

Plastic surface mounted package; 6 leads   **SOT363**

DIMENSIONS (mm are the original dimensions)

UNIT	A	A₁ max	bp	c	D	E	e	e₁	H_E	Lp	Q	v	w	y
mm	1.1 / 0.8	0.1	0.30 / 0.20	0.25 / 0.10	2.2 / 1.8	1.35 / 1.15	1.3	0.65	2.2 / 2.0	0.45 / 0.15	0.25 / 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28
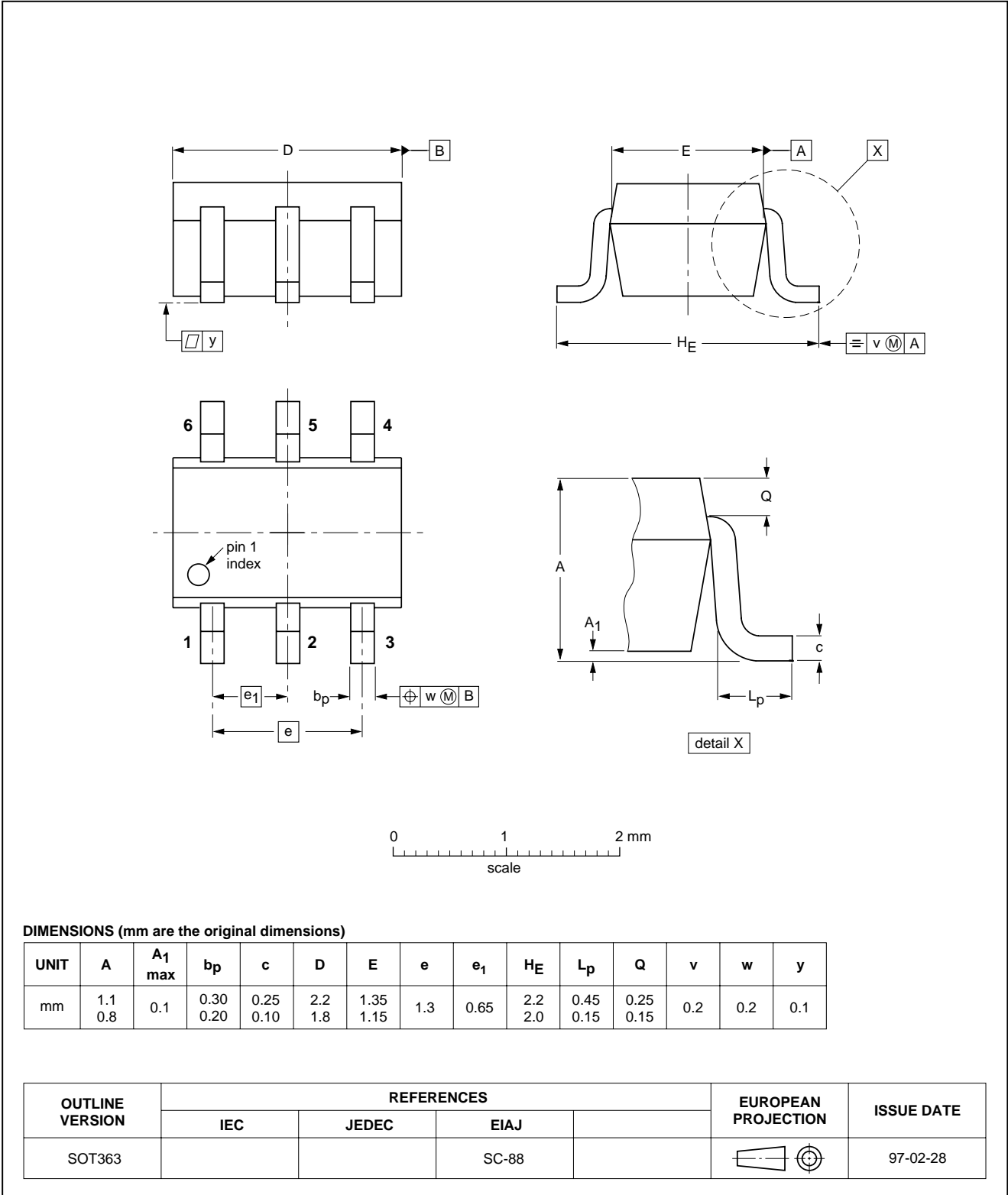
PNP/PNP resistor-equipped transistors;
R1 = 4.7 kΩ, R2 = open

PEMB3; PUMB3

DATA SHEET STATUS

DOCUMENT STATUS[1]	PRODUCT STATUS[2]	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

Notes

1. Please consult the most recently issued document before initiating or completing a design.

2. The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

DISCLAIMERS

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

NXP Semiconductors

Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors. No changes were made to the content, except for the legal definitions and disclaimers.

Contact information

For additional information please visit: **http://www.nxp.com**
For sales offices addresses send e-mail to: **salesaddresses@nxp.com**

founded by

PHILIPS

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

[NXP]():
  [PEMB3,115]() [PUMB3,115]()