

MGSF1N03L, MVGSF1N03L

Power MOSFET

30 V, 2.1 A, Single N-Channel, SOT-23

These miniature surface mount MOSFETs low $R_{DS(on)}$ assure minimal power loss and conserve energy, making these devices ideal for use in space sensitive power management circuitry. Typical applications are dc-dc converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

Features

- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SOT-23 Surface Mount Package Saves Board Space
- AEC-Q101 Qualified and PPAP Capable – MVGSF1N03LT1
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Value	Unit	
Drain-to-Source Voltage		V_{DSS}	30	V	
Gate-to-Source Voltage		V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JL}$	Steady State	I_D	$T_A = 25^\circ\text{C}$	2.1	A
			$T_A = 85^\circ\text{C}$	1.5	
Power Dissipation $R_{\theta JL}$	Steady State	$T_A = 25^\circ\text{C}$	P_D	0.69	W
Continuous Drain Current (Note 1)	Steady State	I_D	$T_A = 25^\circ\text{C}$	1.6	A
			$T_A = 85^\circ\text{C}$	1.2	
Power Dissipation (Note 1)		$T_A = 25^\circ\text{C}$	P_D	0.42	W
Pulsed Drain Current	$t_p = 10 \mu\text{s}$	I_{DM}	6.0	A	
ESD Capability (Note 3)	$C = 100 \text{ pF}$, $R_S = 1500 \Omega$	ESD	125	V	
Operating Junction and Storage Temperature		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$	
Source Current (Body Diode)		I_S	2.1	A	
Lead Temperature for Soldering Purposes (1/8" from case for 10 sec)		T_L	260	$^\circ\text{C}$	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Foot – Steady State	$R_{\theta JL}$	180	$^\circ\text{C/W}$
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	300	
Junction-to-Ambient – $t < 10 \text{ s}$ (Note 1)	$R_{\theta JA}$	250	
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	400	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface-mounted on FR4 board using 650 mm², 1 oz. Cu pad size.
2. Surface-mounted on FR4 board using 50 mm², 1 oz. Cu pad size.
3. ESD Rating Information: HBM Class 0.

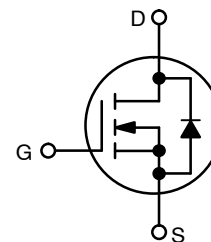


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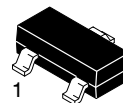
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
30 V	80 m Ω @ 10 V	2.1 A
	125 m Ω @ 4.5 V	

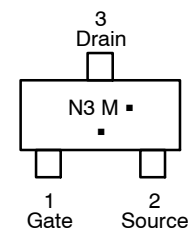
N-Channel



MARKING DIAGRAM/ PIN ASSIGNMENT



SOT-23
CASE 318
STYLE 21



- N3 = Specific Device Code
- M = Date Code*
- = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
MGSF1N03LT1G	SOT-23 Pb-Free	3000 / Tape & Reel
MGSF1N03LT3G	SOT-23 (Pb-Free)	10000 / Tape & Reel
MVGSF1N03LT1G	SOT-23 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

MGSF1N03L, MVGSF1N03L

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit	
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 10\ \mu\text{Adc}$)	$V_{(BR)DSS}$	30	-	-	Vdc	
Zero Gate Voltage Drain Current ($V_{DS} = 30\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$) ($V_{DS} = 30\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$, $T_J = 125^\circ\text{C}$)	I_{DSS}	-	-	1.0 10	μAdc	
Gate-Body Leakage Current ($V_{GS} = \pm 20\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	-	-	± 100	nAdc	
ON CHARACTERISTICS (Note 4)						
Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 250\ \mu\text{Adc}$)	$V_{GS(th)}$	1.0	1.7	2.4	Vdc	
Static Drain-to-Source On-Resistance ($V_{GS} = 10\text{ Vdc}$, $I_D = 1.2\text{ Adc}$) ($V_{GS} = 4.5\text{ Vdc}$, $I_D = 1.0\text{ Adc}$)	$r_{DS(on)}$	-	0.08 0.125	0.10 0.145	Ω	
DYNAMIC CHARACTERISTICS						
Input Capacitance	($V_{DS} = 5.0\text{ Vdc}$)	C_{iss}	-	140	-	pF
Output Capacitance	($V_{DS} = 5.0\text{ Vdc}$)	C_{oss}	-	100	-	
Transfer Capacitance	($V_{DG} = 5.0\text{ Vdc}$)	C_{rss}	-	40	-	
SWITCHING CHARACTERISTICS (Note 5)						
Turn-On Delay Time	($V_{DD} = 15\text{ Vdc}$, $I_D = 1.0\text{ Adc}$, $R_L = 50\ \Omega$)	$t_{d(on)}$	-	2.5	-	ns
Rise Time		t_r	-	1.0	-	
Turn-Off Delay Time		$t_{d(off)}$	-	16	-	
Fall Time		t_f	-	8.0	-	
Gate Charge (See Figure 6)		Q_T	-	6000	-	pC
SOURCE-DRAIN DIODE CHARACTERISTICS						
Continuous Current	I_S	-	-	0.6	A	
Pulsed Current	I_{SM}	-	-	0.75		
Forward Voltage (Note 5)	V_{SD}	-	0.8	-	V	

4. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.
 5. Switching characteristics are independent of operating junction temperature.

TYPICAL ELECTRICAL CHARACTERISTICS

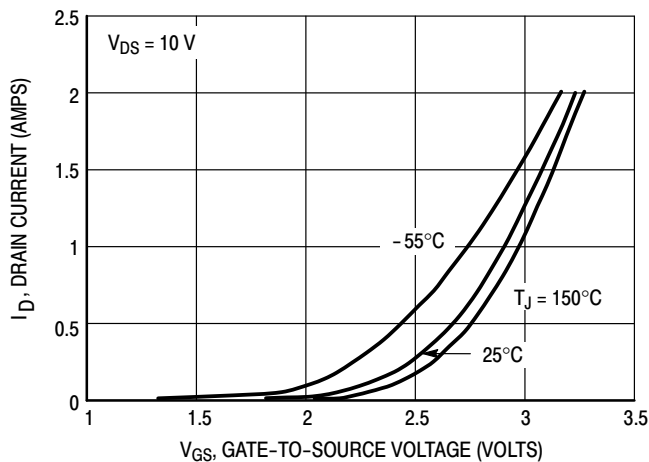


Figure 1. Transfer Characteristics

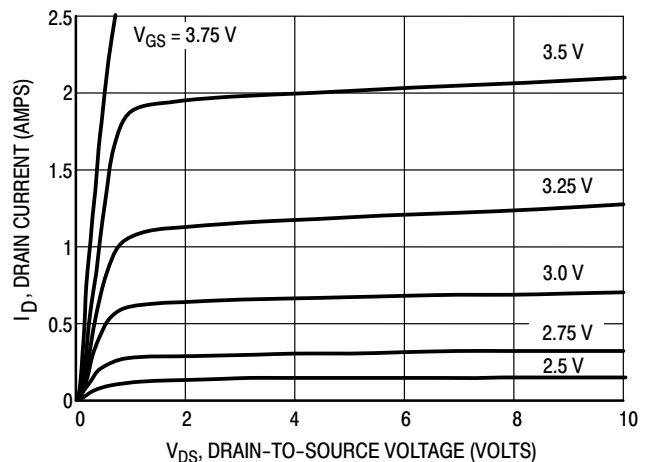


Figure 2. On-Region Characteristics

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TYPICAL ELECTRICAL CHARACTERISTICS

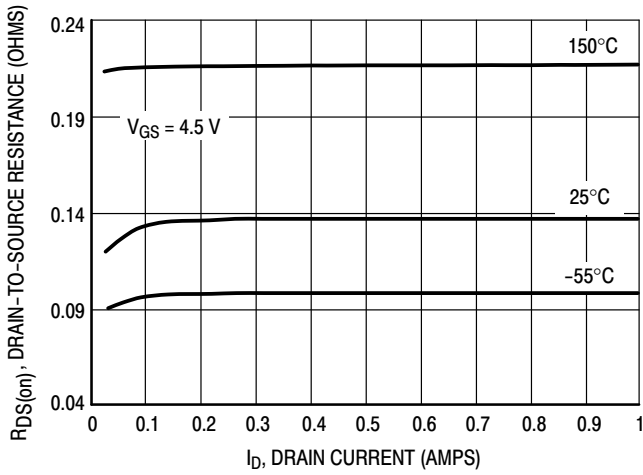


Figure 3. On-Resistance versus Drain Current

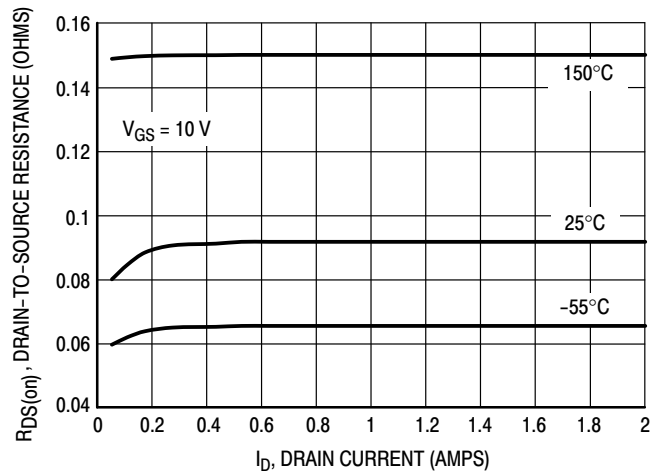


Figure 4. On-Resistance versus Drain Current

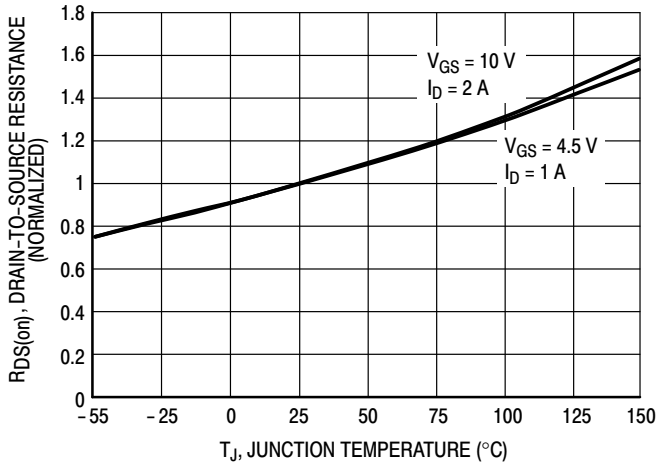


Figure 5. On-Resistance Variation with Temperature

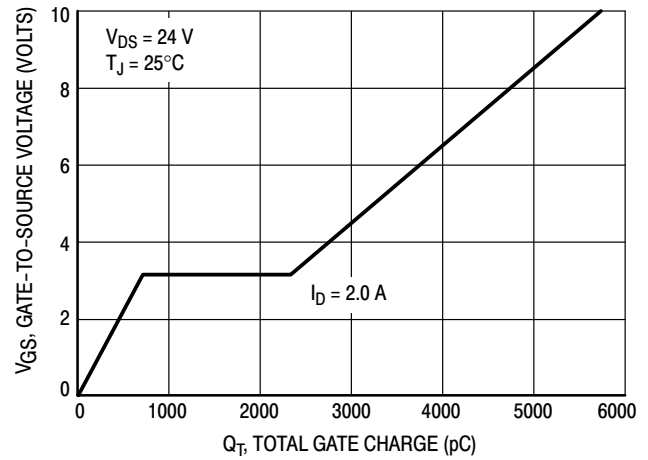


Figure 6. Gate Charge

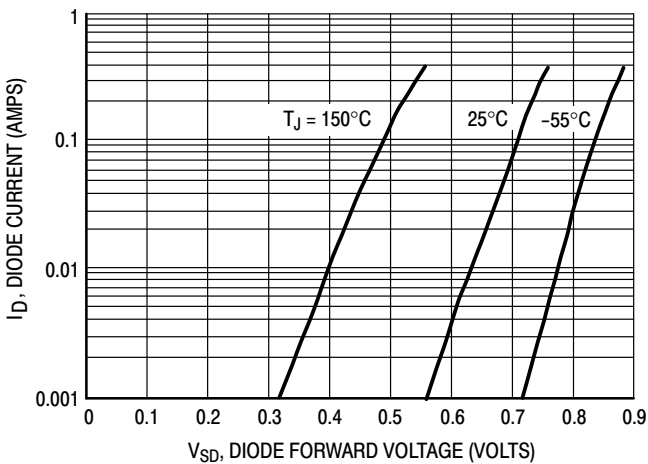


Figure 7. Body Diode Forward Voltage

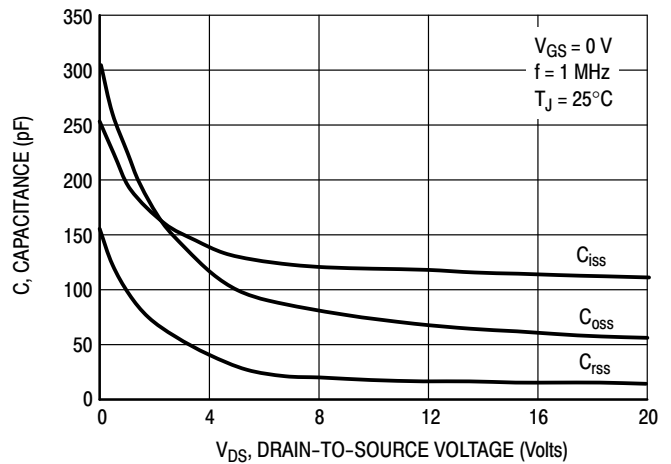


Figure 8. Capacitance

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TYPICAL ELECTRICAL CHARACTERISTICS

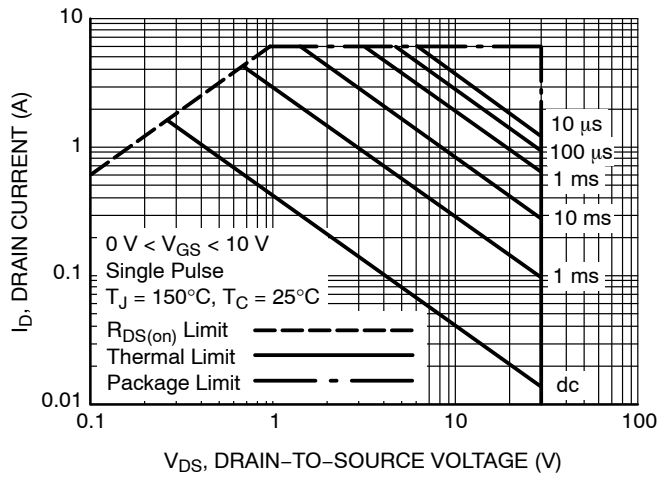


Figure 9. Maximum Rated Forward Biased Safe Operating Area

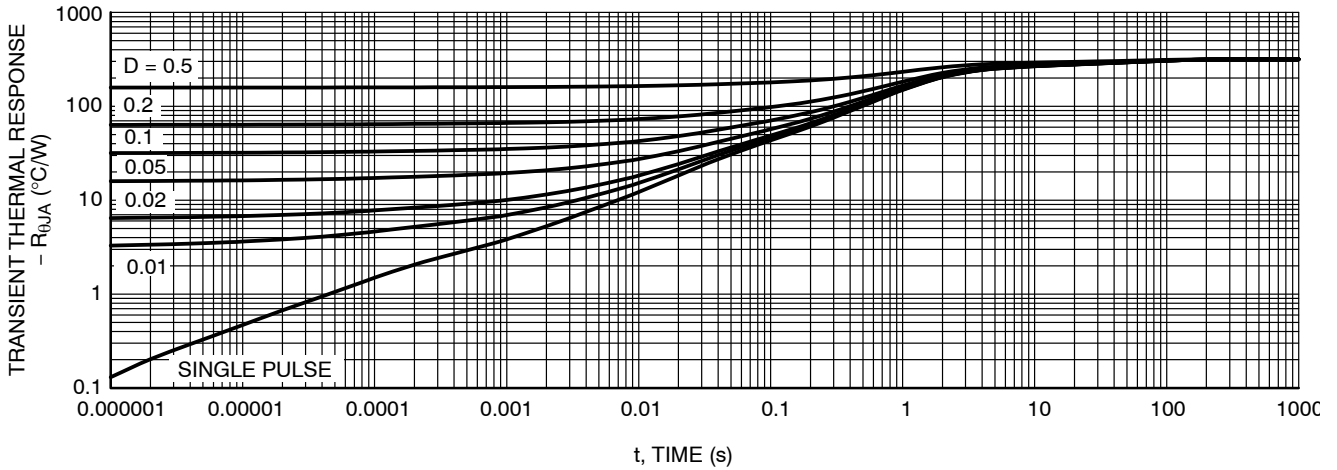
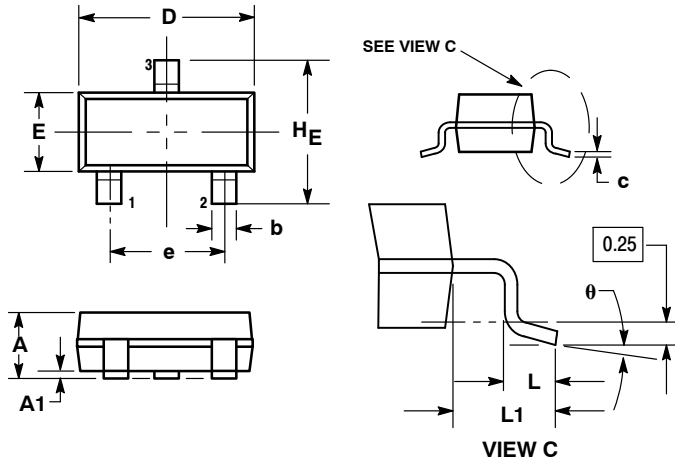


Figure 10. Thermal Response

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PACKAGE DIMENSIONS

SOT-23 (TO-236)
CASE 318-08
ISSUE AP



NOTES:

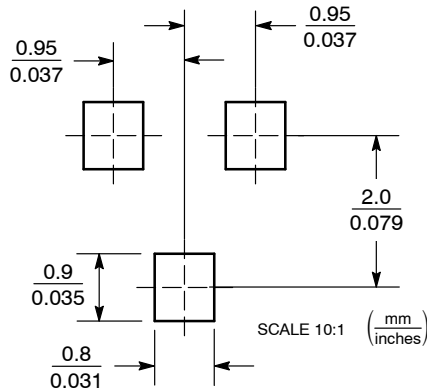
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1.00	1.11	0.035	0.040	0.044
A1	0.01	0.06	0.10	0.001	0.002	0.004
b	0.37	0.44	0.50	0.015	0.018	0.020
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
e	1.78	1.90	2.04	0.070	0.075	0.081
L	0.10	0.20	0.30	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.40	2.64	0.083	0.094	0.104
theta	0°	---	10°	0°	---	10°

STYLE 21:

1. GATE
2. SOURCE
3. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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