# ESDA6V1U1

Application Specific Discretes
A.S.D.

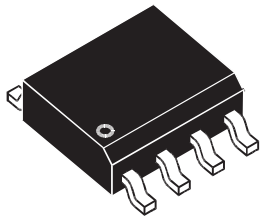
TRANSIL ARRAY
FOR ESD PROTECTION

## APPLICATIONS

Where transient overvoltage protection in ESD sensitive equipment is required, such as :

- COMPUTERS
- PRINTERS
- COMMUNICATION SYSTEMS
- GSM HANDSETS AND ACCESSORIES
- CAR RADIO

It is particulary recommended for parallel port protection where the line interface withstands only 2 kV ESD surge.

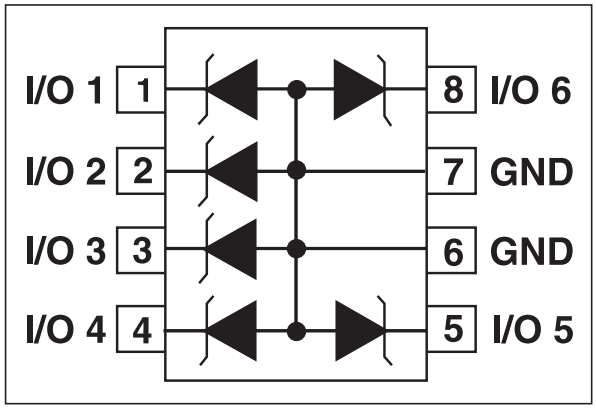


**SO-8**

## FEATURES

- 6 UNIDIRECTIONAL TRANSIL FUNCTIONS
- LOW LEAKAGE CURRENT: $I_R$ max. < 2 µA
- 200 W PEAK PULSE POWER (8/20 µs)

## FUNCTIONAL DIAGRAM




## DESCRITION

The ESDA6V1U1 is a monolithic voltage suppressor designed to protect components which are connected to data and transmission lines against ESD.

It clamps the voltage just above the logic level supply for positive transients, and to a diode drop below ground for negative transients.

## BENEFITS

High ESD protection level : up to 25 kV

High integration

Suitable for high density boards

## COMPLIES WITH THE FOLLOWING STANDARDS :

IEC61000-4-2 : level 4

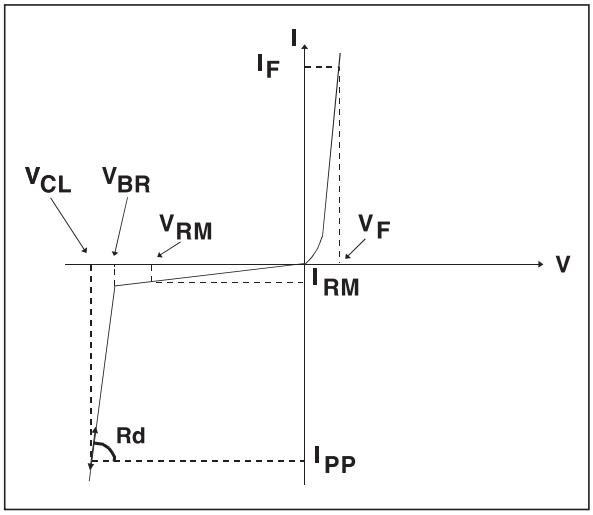
MIL STD 883C-Method 3015-6 : class3
(human body model)

**ABSOLUTE MAXIMUM RATINGS** ($T_{amb}$ = 25°C)

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{PP}$ | Electrostatic discharge<br>MIL STD 883C - Method 3015-6 | 25 | kV |
| $P_{PP}$ | Peak pulse power (8/20µs) | 200 | W |
| $T_{stg}$<br>$T_j$ | Storage temperature range<br>Maximum junction temperature | - 55 to + 150<br>125 | °C<br>°C |
| $T_L$ | Maximum lead temperature for soldering during 10s | 260 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_{amb}$ = 25°C)

| Symbol | Parameter |
|---|---|
| $V_{RM}$ | Stand-off voltage |
| $V_{BR}$ | Breakdown voltage |
| $V_{CL}$ | Clamping voltage |
| $I_{RM}$ | Leakage current |
| $I_{PP}$ | Peak pulse current |
| $\alpha T$ | Voltage temperature coefficient |
| C | Capacitance |
| Rd | Dynamic resistance |
| $V_F$ | Forward voltage drop |




| Types | $V_{BR}$ @ $I_R$ | | | $I_{RM}$ @ $V_{RM}$ | | Rd | αT | C | $V_F$ @ $I_F$ | |
|---|---|---|---|---|---|---|---|---|---|---|
| | min. | max. | | max. | | typ.<br>note 1 | max.<br>note 2 | typ.<br>0V bias | max. | |
| | V | V | mA | µA | V | Ω | $10^{-4}$/°C | pF | V | mA |
| ESDA6V1U1 | 6.1 | 7.2 | 1 | 2 | 5 | 0.5 | 6 | 100 | 1.5 | 200 |

**note 1** : Square pulse, Ipp = 25A, tp=2.5µs.
**note 2** : $\Delta V_{BR} = \alpha T^* (Tamb - 25°C) * V_{BR} (25°C)$

## CALCULATION OF THE CLAMPING VOLTAGE

### USE OF THE DYNAMIC RESISTANCE

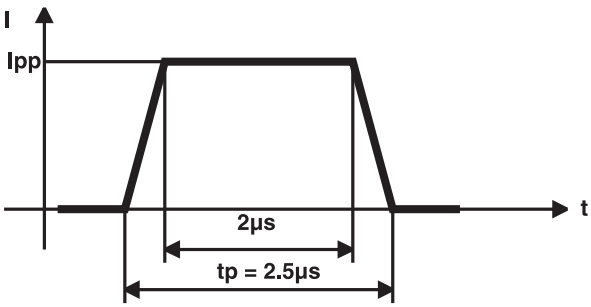
The ESDA family has been designed to clamp fast spikes like ESD. Generally the PCB designers need to calculate easily the clamping voltage $V_{CL}$. This is why we give the dynamic resistance in addition to the classical parameters. The voltage across the protection cell can be calculated with the following formula:

$$V_{CL} = V_{BR} + Rd\ I_{PP}$$

Where Ipp is the peak current through the ESDA cell.

### DYNAMIC RESISTANCE MEASUREMENT

The short duration of the ESD has led us to prefer a more adapted test wave, as below defined, to the classical 8/20µs and 10/1000µs surges.




2.5µs duration measurement wave.

As the value of the dynamic resistance remains stable for a surge duration lower than 20µs, the 2.5µs rectangular surge is well adapted. In addition both rise and fall times are optimized to avoid any parasitic phenomenon during the measurement of Rd.

**Fig. 1 :** Peak power dissipation versus initial junction temperature.

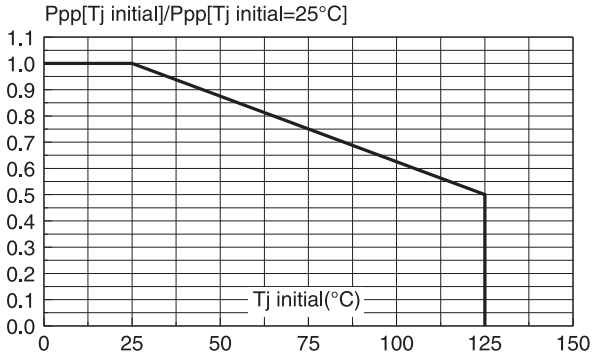



**Fig. 2 :** Peak pulse power versus exponential pulse duration (Tj initial = 25 °C).

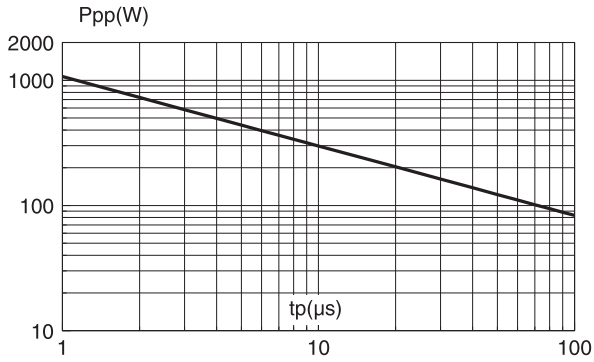



**Fig. 3 :** Clamping voltage versus peak pulse current (Tj initial = 25 °C).

Rectangular waveform tp = 2.5 µs.

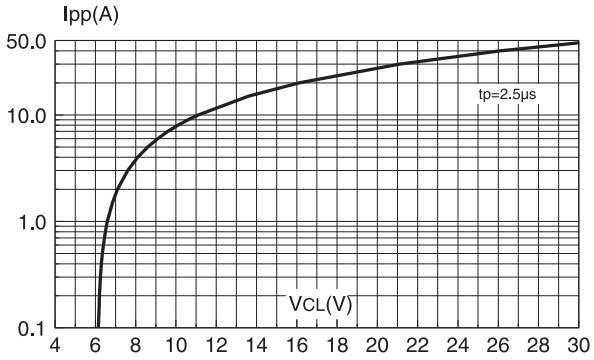



**Fig. 4 :** Capacitance versus reverse applied voltage (typical values).

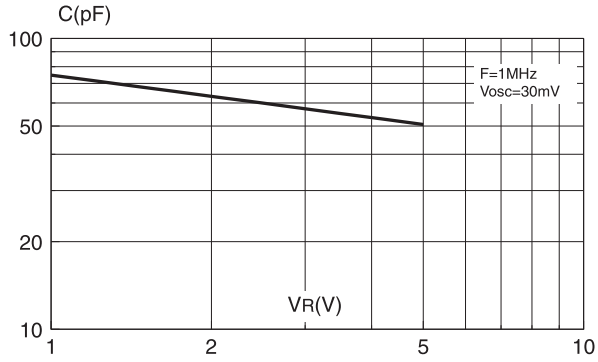



**Fig. 5 :** Relative variation of leakage current versus junction temperature (typical values).

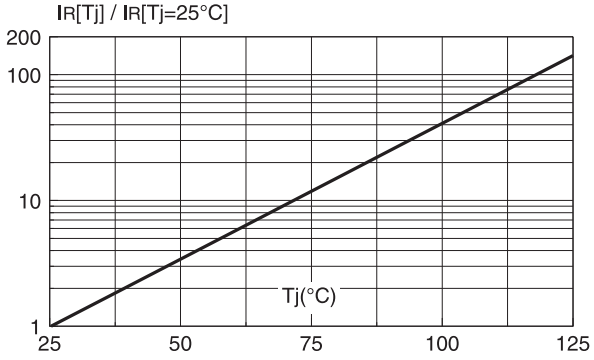
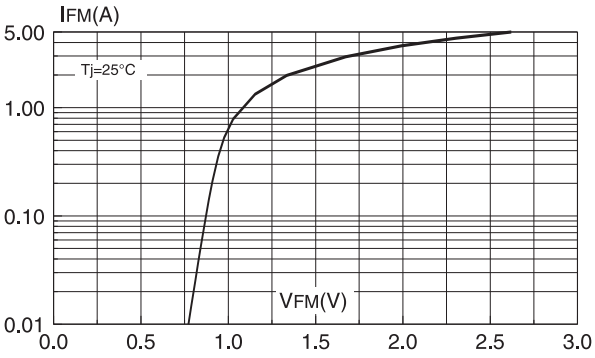
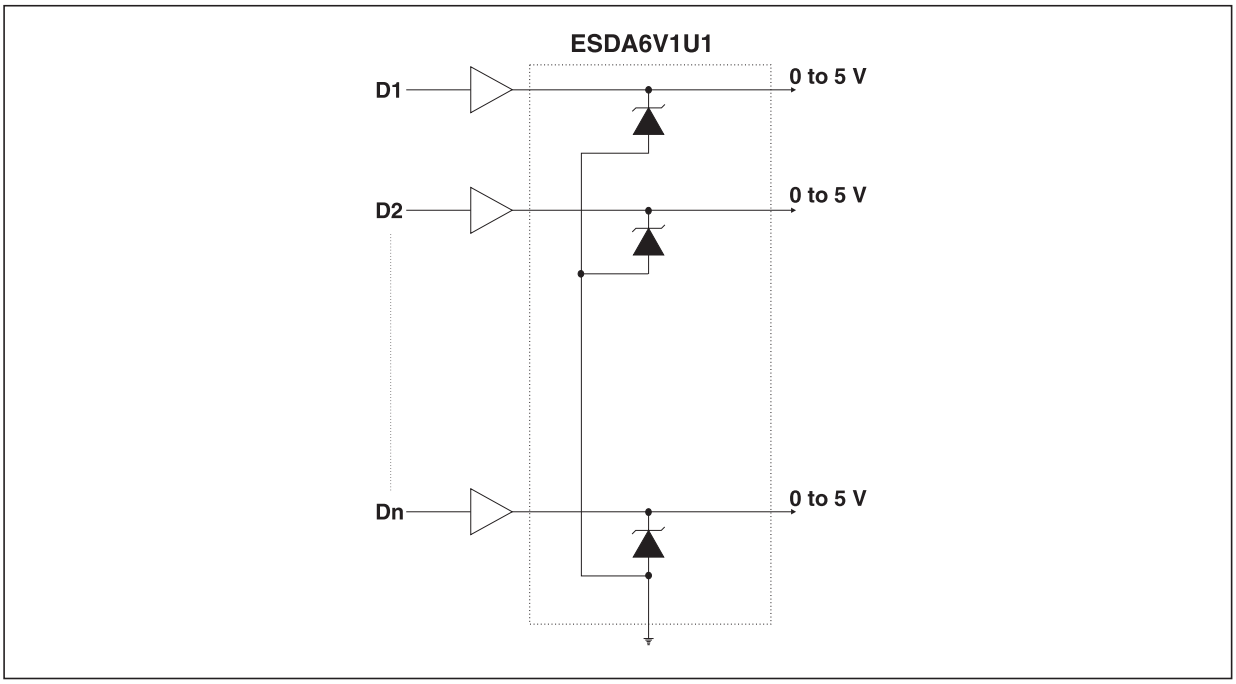


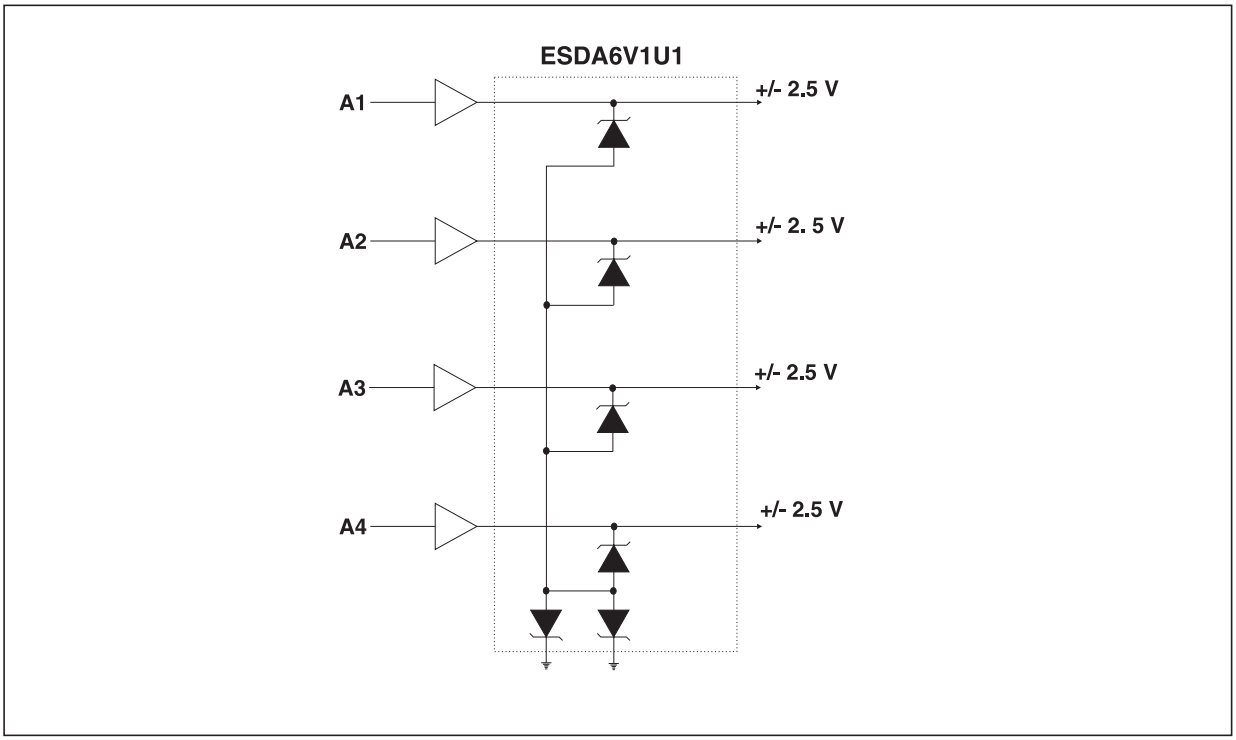

**Fig. 6 :** Peak forward voltage drop versus peak forward current (typical values).



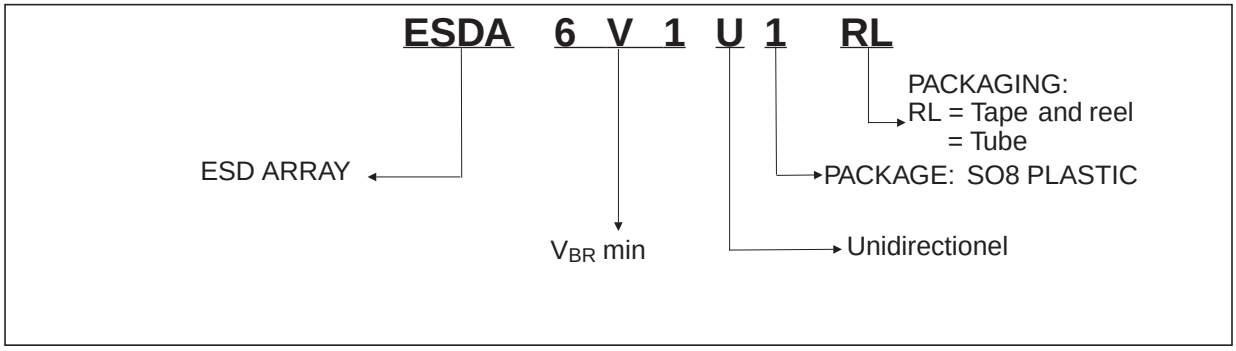
**APPLICATION EXAMPLE :** Protection of logic-level signals.




**APPLICATION EXAMPLE :** Protection of symmetrical signals.
**Note :** Capacitance value between any I/O pin and Ground is divided by 2.



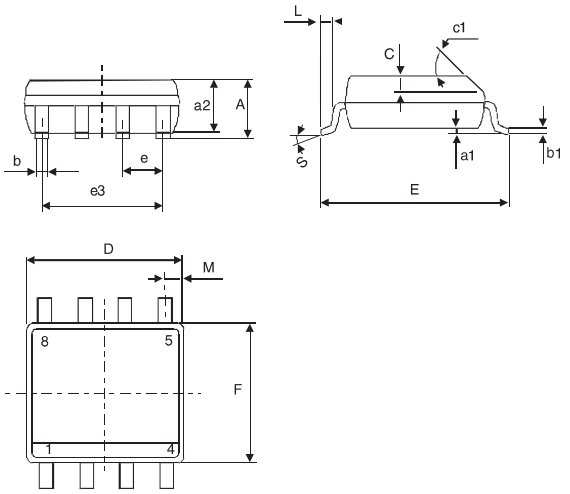
## ORDER CODE




**MARKING :** Logo, Date Code, E6V1U1

## PACKAGE MECHANICAL DATA

SO-8 Plastic




| REF. | DIMENSIONS | | | | | |
|---|---|---|---|---|---|---|
| | Millimetres | | | Inches | | |
| | Min. | Typ. | Max. | Min. | Typ. | Max. |
| A | | | 1.75 | | | 0.069 |
| a1 | 0.1 | | 0.25 | 0.004 | | 0.010 |
| a2 | | | 1.65 | | | 0.065 |
| b | 0.35 | | 0.48 | 0.014 | | 0.019 |
| b1 | 0.19 | | 0.25 | 0.007 | | 0.010 |
| C | | 0.50 | | | 0.020 | |
| c1 | 45° (typ) | | | | | |
| D | 4.8 | | 5.0 | 0.189 | | 0.197 |
| E | 5.8 | | 6.2 | 0.228 | | 0.244 |
| e | | 1.27 | | | 0.050 | |
| e3 | | 3.81 | | | 0.150 | |
| F | 3.8 | | 4.0 | 0.15 | | 0.157 |
| L | 0.4 | | 1.27 | 0.016 | | 0.050 |
| M | | | 0.6 | | | 0.024 |
| S | 8° (max) | | | | | |

**Packaging :** Preferred packaging is tape and reel.

**Weight :** 0.08g.

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