

N-channel 100 V, 0.027 Ω typ., 8 A, STripFET™ VII DeepGATE™ Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

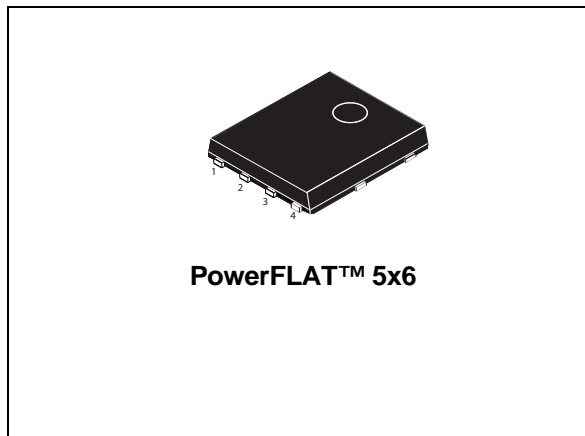
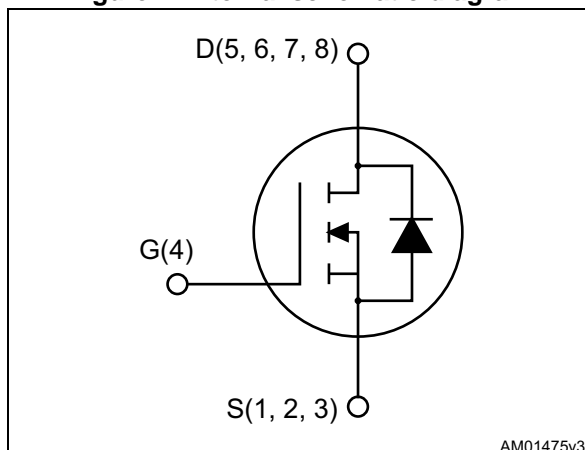


Figure 1. Internal schematic diagram



Features

| Order code | V_{DS} | $R_{DS(on)}$ max. | I_D | P_{TOT} |
|------------|----------|-------------------|-------|----------------------|
| STL30N10F7 | 100 V | 0.035 Ω | 8 A | 4.8 W ⁽¹⁾ |

 1. The value is rated according to $R_{thj-pcb}$.

- Ultra low on-resistance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the 7th generation of STripFET™ DeepGATE™ technology, with a new gate structure. The resulting Power MOSFET exhibits the lowest $R_{DS(on)}$ in all packages.

Table 1. Device summary

| Order code | Marking | Package | Packaging |
|------------|---------|----------------|---------------|
| STL30N10F7 | 30N10F7 | PowerFLAT™ 5x6 | Tape and reel |

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1 Electrical ratings

Table 2. Absolute maximum ratings

| Symbol | Parameter | Value | Unit |
|--------------------|--|------------|------------------|
| V_{DS} | Drain-source voltage | 100 | V |
| V_{GS} | Gate-source voltage | ± 20 | V |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$ | 30 | A |
| $I_D^{(1)}$ | Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$ | 18.2 | A |
| $I_D^{(1)(3)}$ | Drain current (pulsed) | 120 | A |
| $I_D^{(2)}$ | Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$ | 8 | A |
| $I_D^{(2)}$ | Drain current (continuous) at $T_{pcb}=100\text{ }^\circ\text{C}$ | 5.2 | A |
| $I_{DM}^{(2)(3)}$ | Drain current (pulsed) | 32 | A |
| $P_{TOT}^{(1)}$ | Total dissipation at $T_C = 25\text{ }^\circ\text{C}$ | 75 | W |
| $P_{TOT}^{(2)}$ | Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$ | 4.8 | W |
| T_J T_{stg} | Operating junction temperature Storage temperature | -55 to 175 | $^\circ\text{C}$ |

1. This value is rated according to R_{thj-c} .
2. This value is rated according to $R_{thj-pcb}$.
3. Pulse width limited by safe operating area.

Table 3. Thermal data

| Symbol | Parameter | Value | Unit |
|---------------------|---------------------------------------|-------|--------------------|
| $R_{thj-case}$ | Thermal resistance junction-case max. | 2 | $^\circ\text{C/W}$ |
| $R_{thj-pcb}^{(1)}$ | Thermal resistance junction-pcb | 31.3 | $^\circ\text{C/W}$ |

1. When mounted on FR-4 board of 1 inch², 2oz Cu, t < 10 sec.

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 4. On /off states

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---------------|-----------------------------------|--|------|-------|-------|---------------|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$ | 100 | | | V |
| I_{DSS} | Zero gate voltage drain current | $V_{GS} = 0, V_{DS} = 100\text{ V}$ | | | 10 | μA |
| | | $V_{GS} = 0, V_{DS} = 100\text{ V}, T_C = 125\text{ °C}$ | | | 100 | μA |
| I_{GSS} | Gate-body leakage current | $V_{DS} = 0, V_{GS} = +20\text{ V}$ | | | 100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | 2.5 | | 4.5 | V |
| $R_{DS(on)}$ | Static drain-source on-resistance | $V_{GS} = 10\text{ V}, I_D = 4\text{ A}$ | | 0.027 | 0.035 | Ω |

Table 5. Dynamic

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|------------|------------------------------|--|------|------|------|------|
| C_{iss} | Input capacitance | $V_{DS} = 50\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$ | - | 920 | - | pF |
| C_{oss} | Output capacitance | | - | 215 | - | pF |
| C_{riss} | Reverse transfer capacitance | | - | 19 | - | pF |
| Q_g | Total gate charge | $V_{DD} = 50\text{ V}, I_D = 8\text{ A}, V_{GS} = 10\text{ V}$ (see Figure 14) | - | 14 | - | nC |
| Q_{gs} | Gate-source charge | | - | 7 | - | nC |
| Q_{gd} | Gate-drain charge | | - | 3 | - | nC |

Table 6. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|--------------|---------------------|---|------|------|------|------|
| $t_{d(on)}$ | Turn-on delay time | $V_{DD} = 50\text{ V}, I_D = 4\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ (see Figure 13) | - | 9.8 | - | ns |
| t_r | Rise time | | - | 14 | - | ns |
| $t_{d(off)}$ | Turn-off delay time | | - | 14.8 | - | ns |
| t_f | Fall time | | - | 4.6 | - | ns |

Table 7. Source-drain diode

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|-----------------|-------------------------------|--|------|------|------|------|
| I_{SD} | Source-drain current | | - | | 8 | A |
| $I_{SDM}^{(1)}$ | Source-drain current (pulsed) | | - | | 32 | A |
| $V_{SD}^{(2)}$ | Forward on voltage | $I_{SD} = 8 \text{ A}$, $V_{GS} = 0$ | - | | 1.1 | V |
| t_{rr} | Reverse recovery time | $I_{SD} = 8 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 80 \text{ V}$, $T_J = 150 \text{ }^\circ\text{C}$ | - | 38 | | ns |
| Q_{rr} | Reverse recovery charge | | - | 29 | | nC |
| I_{RRM} | Reverse recovery current | | - | 1.7 | | A |

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

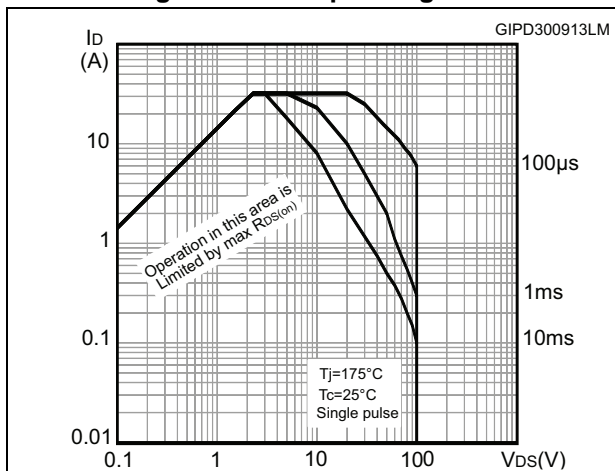


Figure 3. Thermal impedance

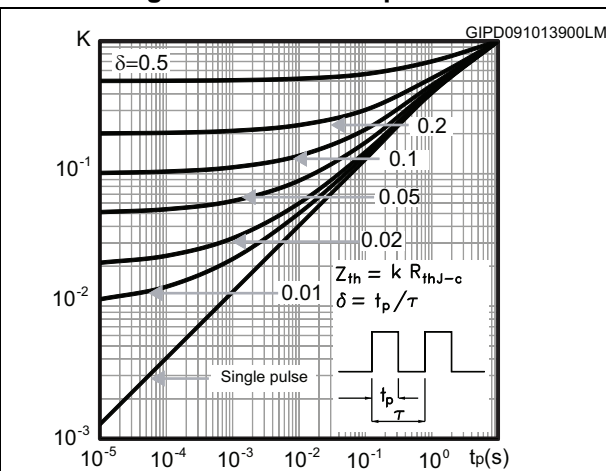


Figure 4. Output characteristics

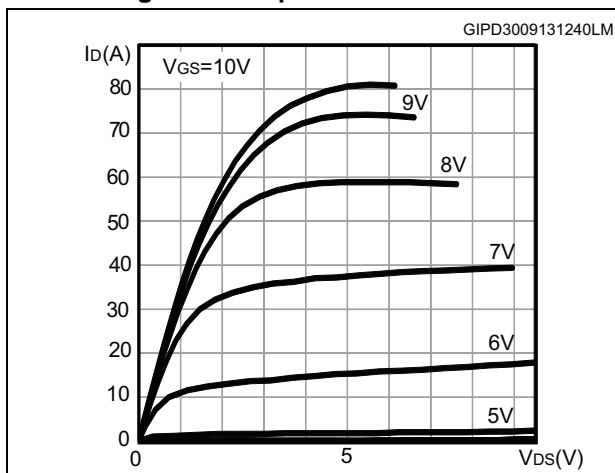


Figure 5. Transfer characteristics

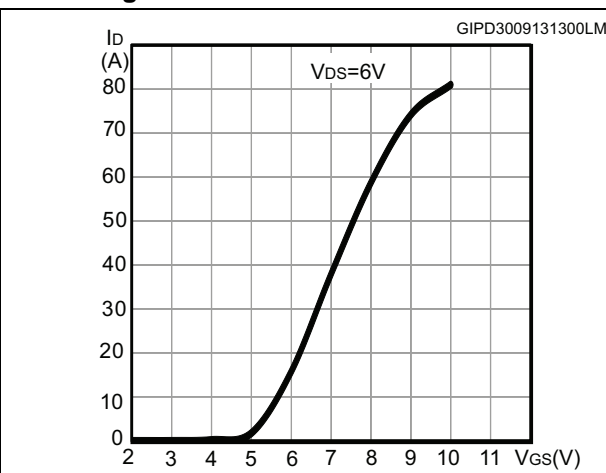


Figure 6. Gate charge vs gate-source voltage

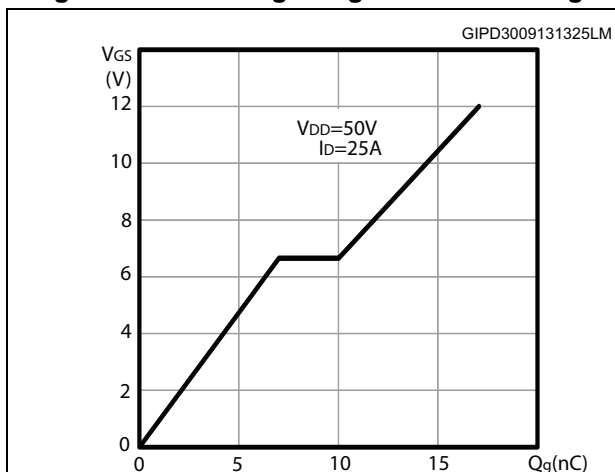


Figure 7. Static drain-source on-resistance

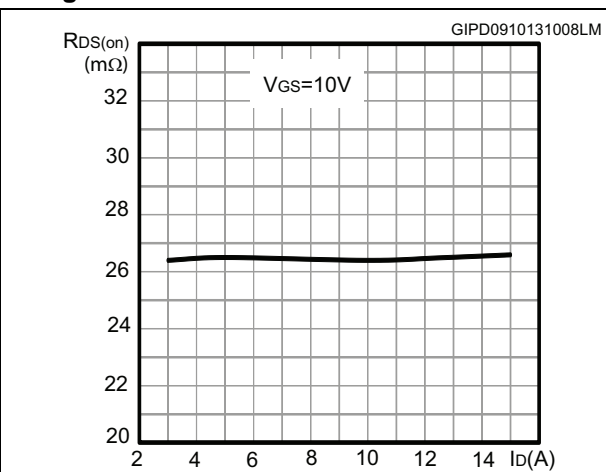


Figure 8. Capacitance variations

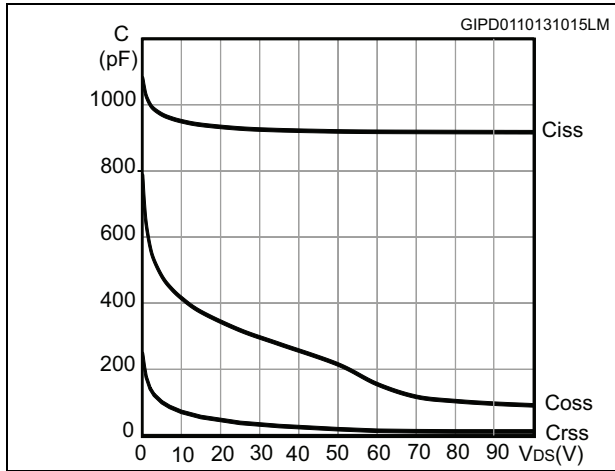


Figure 9. Normalized gate threshold voltage vs temperature

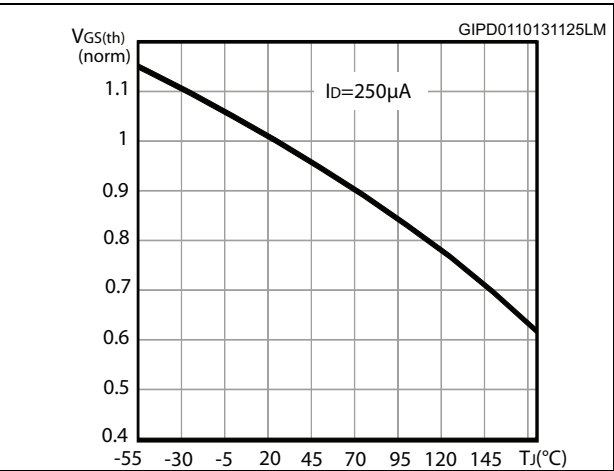


Figure 10. Normalized on-resistance vs temperature

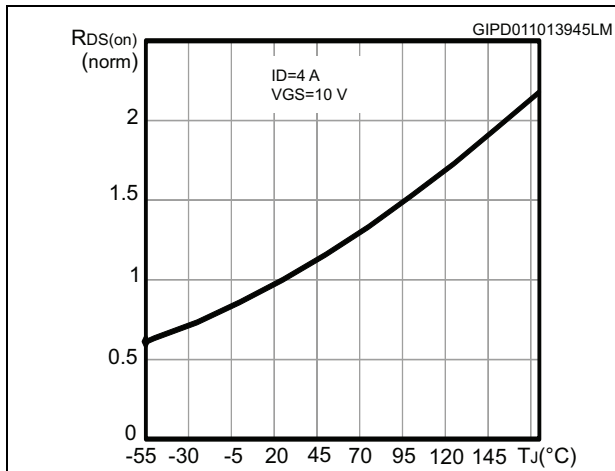


Figure 11. Source-drain diode forward characteristics

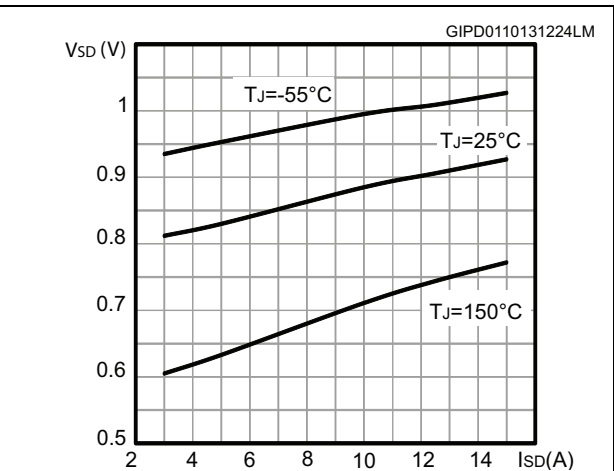
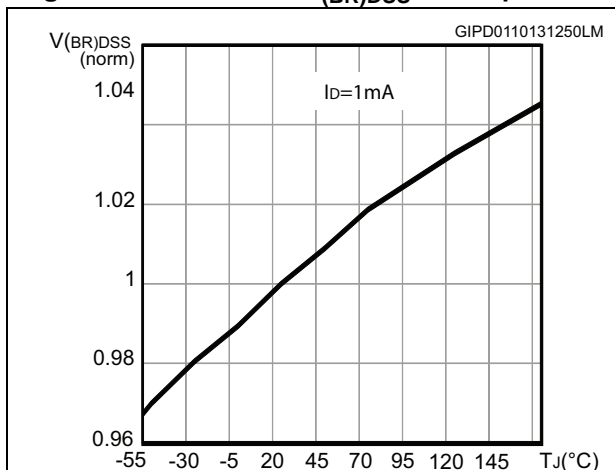


Figure 12. Normalized $V_{(BR)DSS}$ vs temperature



3 Test circuits

Figure 13. Switching times test circuit for resistive load



Figure 14. Gate charge test circuit

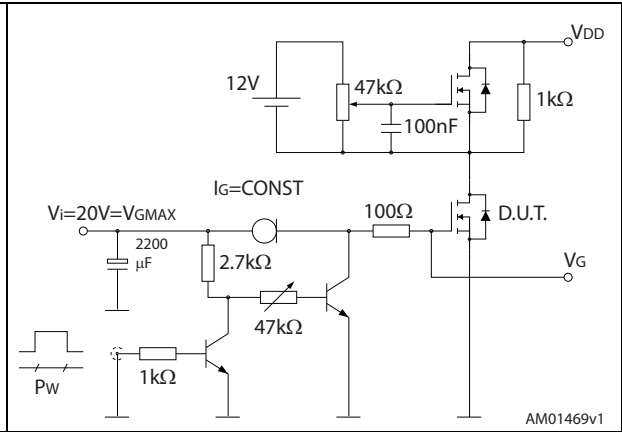


Figure 15. Test circuit for inductive load switching and diode recovery times



Figure 16. Unclamped inductive load test circuit



Figure 17. Unclamped inductive waveform



Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 8. PowerFLAT 5x6 type S-R mechanical data

| Dim. | mm | | |
|------|-------|------|-------|
| | Min. | Typ. | Max. |
| A | 0.80 | | 1.00 |
| A1 | 0.02 | | 0.05 |
| A2 | | 0.25 | |
| b | 0.30 | | 0.50 |
| D | 5.00 | 5.20 | 5.40 |
| E | 5.95 | 6.15 | 6.35 |
| D2 | 4.11 | | 4.31 |
| E2 | 3.50 | | 3.70 |
| e | | 1.27 | |
| L | 0.60 | | 0.80 |
| K | 1.275 | | 1.575 |

Figure 19. PowerFLAT 5x6 type S-R drawings

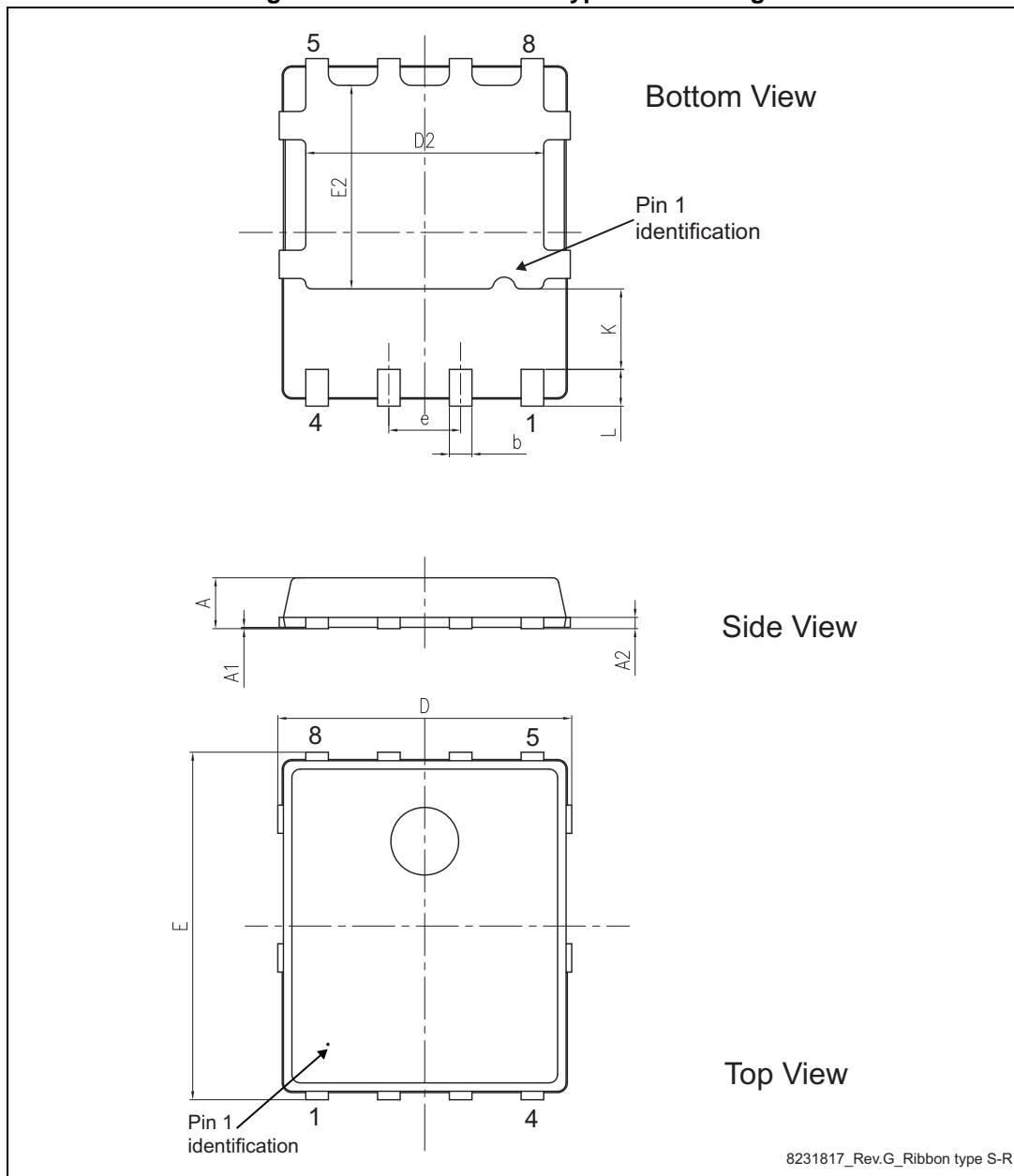
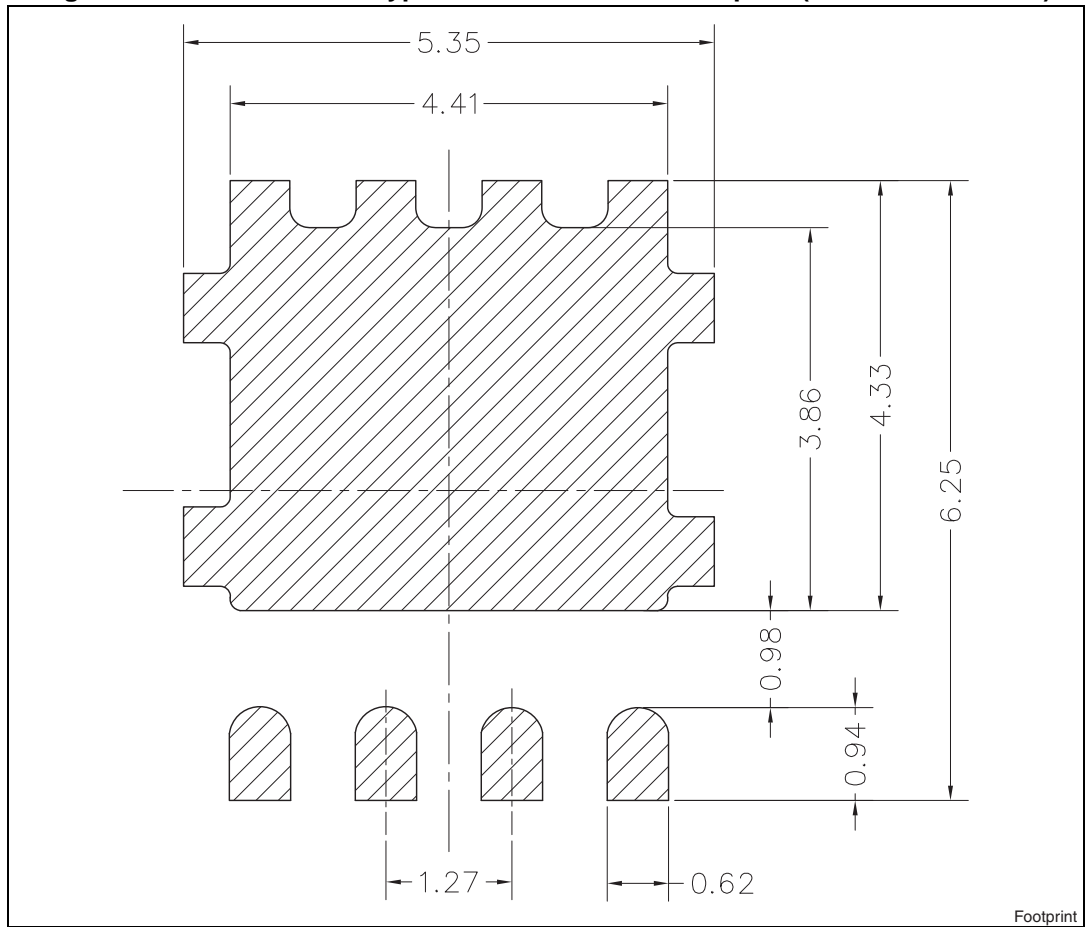


Figure 20. PowerFLAT 5x6 type S-R recommended footprint (dimensions in mm)



5 Packaging mechanical data

Figure 21. PowerFLAT™ 5x6 tape^(a)

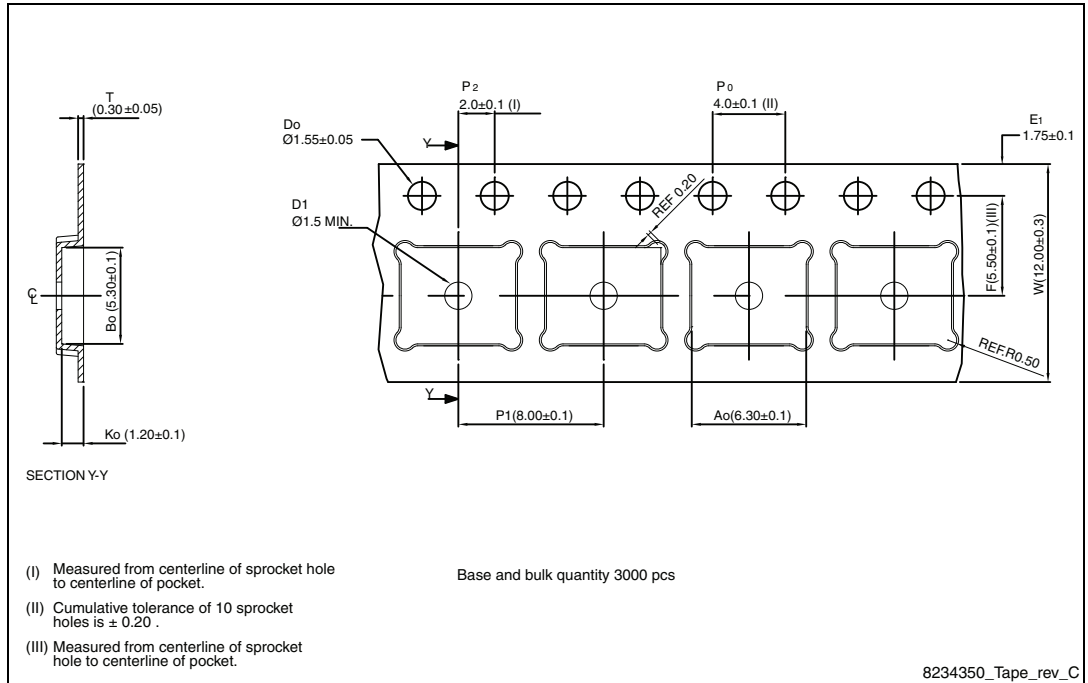
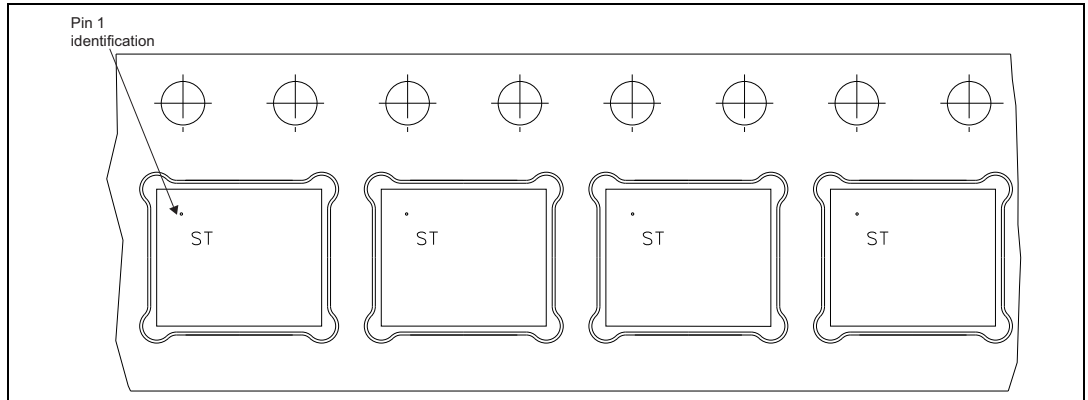
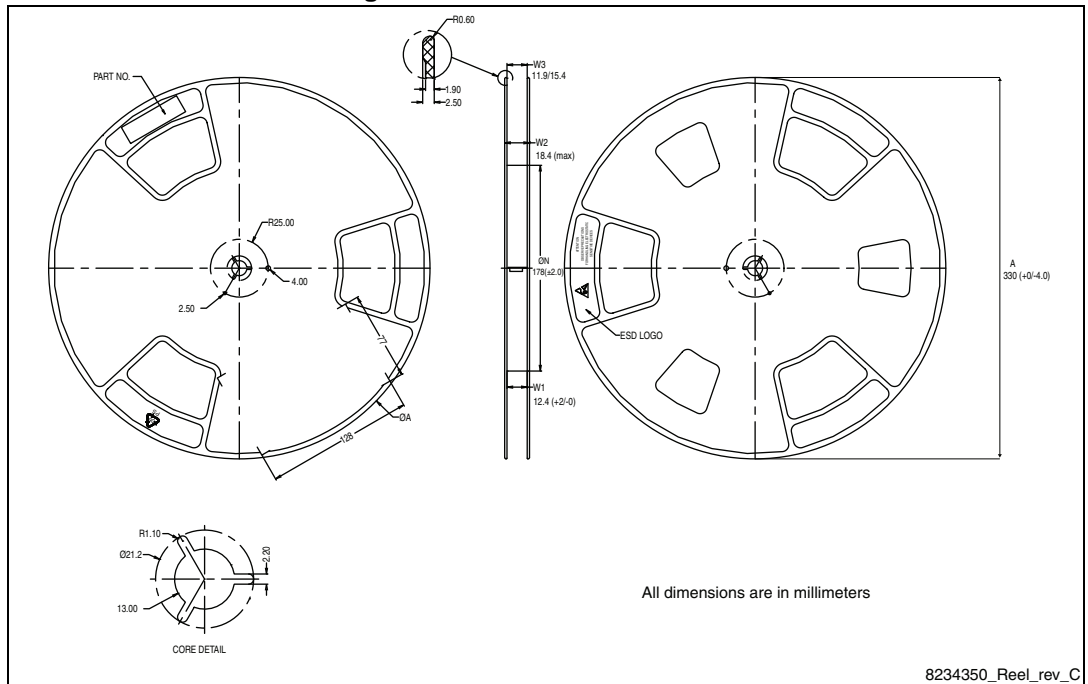


Figure 22. PowerFLAT™ 5x6 package orientation in carrier tape



a. All dimensions are in millimeters.

Figure 23. PowerFLAT™ 5x6 reel



6 Revision history

Table 9. Document revision history

| Date | Revision | Changes |
|-------------|----------|----------------|
| 22-Oct-2013 | 1 | First release. |

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