

## Automotive-grade dual N-channel 60 V, 21 mΩ typ., 32 A STripFET™ F6 Power MOSFET in a PowerFLAT™ 5x6 DI package

Datasheet - production data

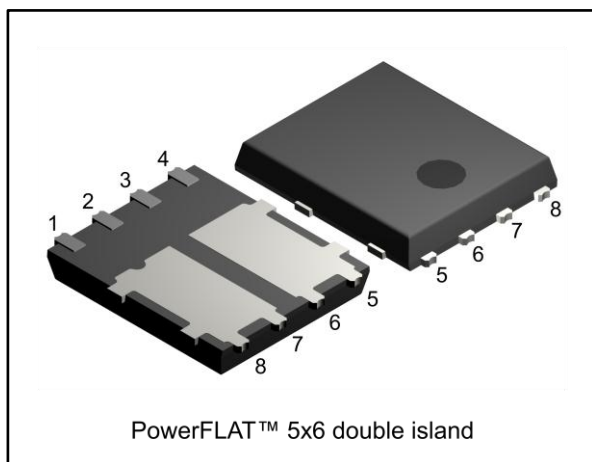
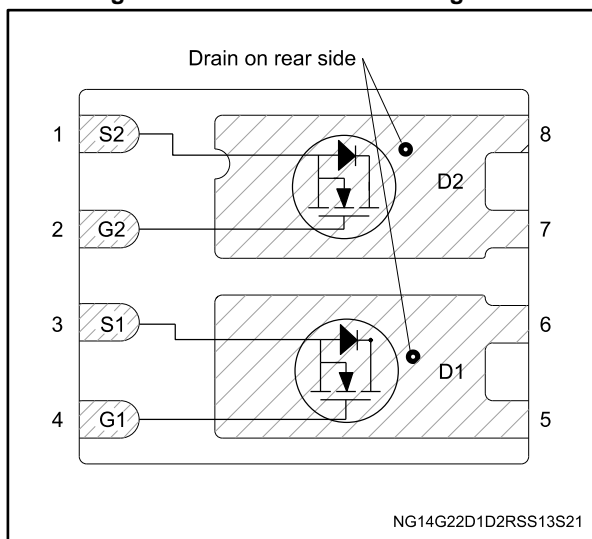


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STL8DN6LF6AG	60 V	27 mΩ	32 A	55 W

- Designed for automotive applications and AEC-Q101 qualified
- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss
- Wettable flank package

### Applications

- Switching applications

### Description

This device is a dual N-channel Power MOSFET developed using the STripFET™ F6 technology with a new trench gate structure. The resulting Power MOSFET exhibits very low R<sub>DS(on)</sub> in all packages.

Table 1: Device summary

Order code	Marking	Package	Packing
STL8DN6LF6AG	8DN6LF6	PowerFLAT™ 5x6 double island	Tape and reel

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	60	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_{case} = 25\text{ }^\circ\text{C}$	32	A
	Drain current (continuous) at $T_{case} = 100\text{ }^\circ\text{C}$	23	
$I_D^{(1)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	9.6	A
	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	6.8	
$I_{DM}^{(1)(2)}$	Drain current (pulsed)	38	A
$I_{DM}^{(2)}$	Drain current (pulsed)	128	A
$P_{TOT}$	Total dissipation at $T_{case} = 25\text{ }^\circ\text{C}$ (one channel active)	55	W
$P_{TOT}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$ (one channel active)	4.8	
$T_{stg}$	Storage temperature	-55 to 175	$^\circ\text{C}$
$T_j$	Operating junction temperature		

**Notes:**

<sup>(1)</sup> When mounted on a 1-inch<sup>2</sup> FR-4, 2 Oz copper board,  $t < 10\text{ s}$ .

<sup>(2)</sup> Pulse width is limited by safe operating area

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	2.7	$^\circ\text{C/W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.3	

**Notes:**

<sup>(1)</sup> When mounted on a 1-inch<sup>2</sup> FR-4, 2 Oz copper board,  $t < 10\text{ s}$ .

**Table 4: Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AV}$	Avalanche current, not repetitive	32	A
$E_{AS}^{(1)}$	Single pulse avalanche energy	120	mJ

**Notes:**

<sup>(1)</sup> starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_D = 38\text{ A}$ ,  $V_{DD} = 43.5\text{ V}$ .

## 2 Electrical characteristics

( $T_{\text{case}} = 25\text{ °C}$  unless otherwise specified)

**Table 5: Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$ , $I_{\text{D}} = 250\text{ }\mu\text{A}$	60			V
$I_{\text{DSS}}$	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$ , $V_{\text{DS}} = 60\text{ V}$			1	$\mu\text{A}$
$I_{\text{GSS}}$	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$ , $V_{\text{GS}} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$ , $I_{\text{D}} = 250\text{ }\mu\text{A}$	1		2.5	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$ , $I_{\text{D}} = 9.6\text{ A}$		21	27	m $\Omega$
		$V_{\text{GS}} = 4.5\text{ V}$ , $I_{\text{D}} = 9.6\text{ A}$		25	31	

**Table 6: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{\text{iss}}$	Input capacitance	$V_{\text{DS}} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{\text{GS}} = 0\text{ V}$	-	1340	-	pF
$C_{\text{oss}}$	Output capacitance		-	90	-	
$C_{\text{riss}}$	Reverse transfer capacitance		-	60	-	
$Q_{\text{g}}$	Total gate charge	$V_{\text{DD}} = 30\text{ V}$ , $I_{\text{D}} = 9.6\text{ A}$ , $V_{\text{GS}} = 10\text{ V}$ (see <a href="#">Figure 14: "Test circuit for gate charge behavior"</a> )	-	27	-	nC
$Q_{\text{gs}}$	Gate-source charge		-	4.6	-	
$Q_{\text{gd}}$	Gate-drain charge		-	4.3	-	

**Table 7: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 30\text{ V}$ , $I_{\text{D}} = 12.5\text{ A}$ , $R_{\text{G}} = 4.7\text{ }\Omega$ , $V_{\text{GS}} = 10\text{ V}$ (see <a href="#">Figure 13: "Test circuit for resistive load switching times"</a> and <a href="#">Figure 18: "Switching time waveform"</a> )	-	9.6	-	ns
$t_{\text{r}}$	Rise time		-	20	-	
$t_{\text{d(off)}}$	Turn-off delay time		-	56	-	
$t_{\text{f}}$	Fall time		-	7	-	

Table 8: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		9.6	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		38	A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$ , $I_{SD} = 9.6\text{ A}$	-		1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 25\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 48\text{ V}$ , $T_j = 25\text{ }^\circ\text{C}$ (see <a href="#">Figure 15: "Test circuit for inductive load switching and diode recovery times"</a> )	-	22.5		ns
$Q_{rr}$	Reverse recovery charge		-	22.2		nC
$I_{RRM}$	Reverse recovery current		-	2.0		A

**Notes:**

(1) Pulse width is limited by safe operating area.

(2) Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

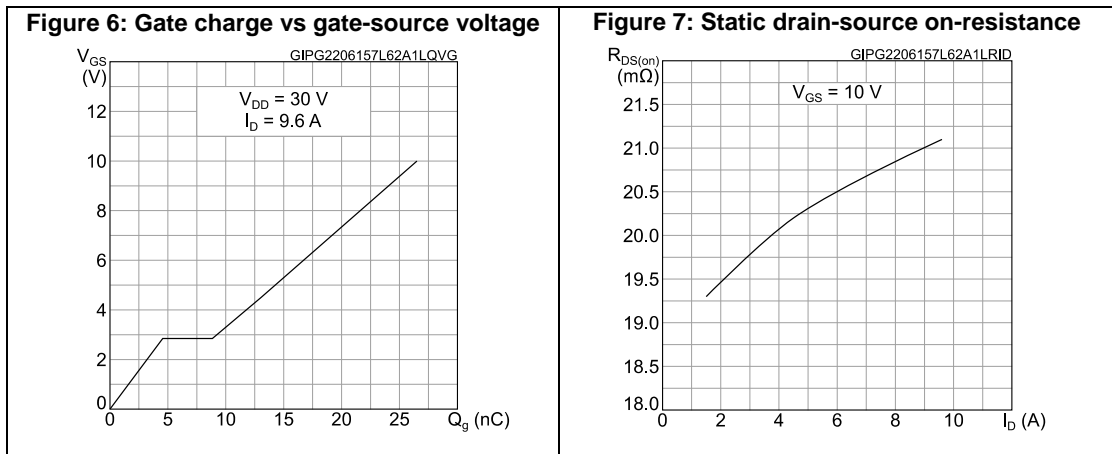
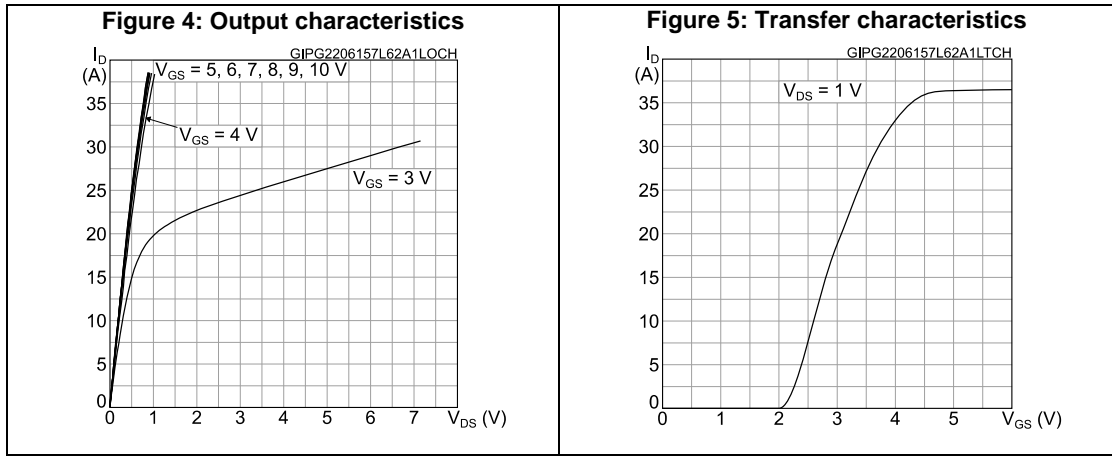
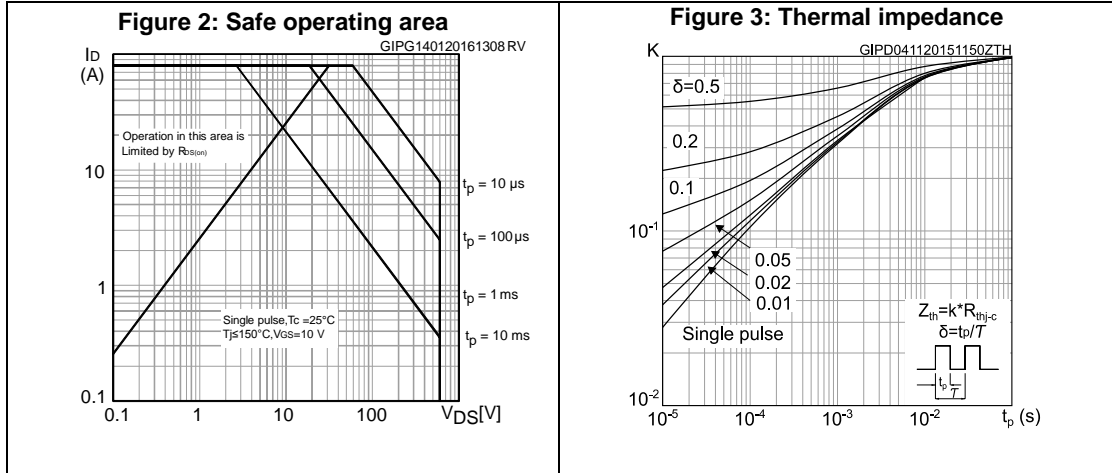


Figure 8: Capacitance variations

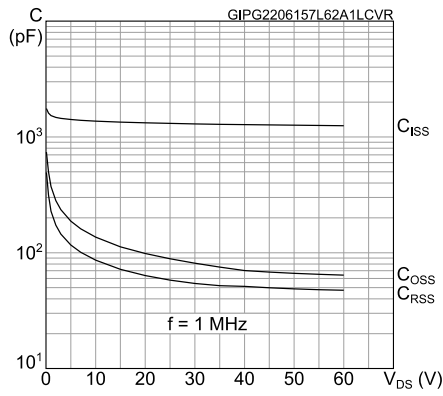


Figure 9: Normalized gate threshold voltage vs temperature

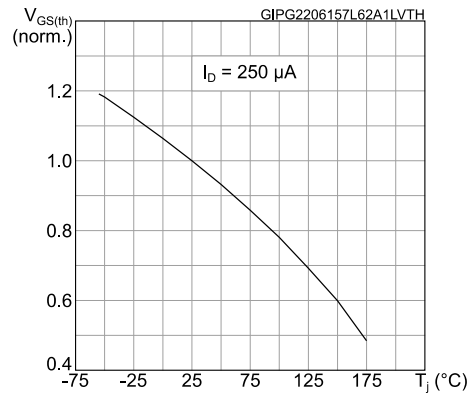


Figure 10: Normalized on-resistance vs temperature

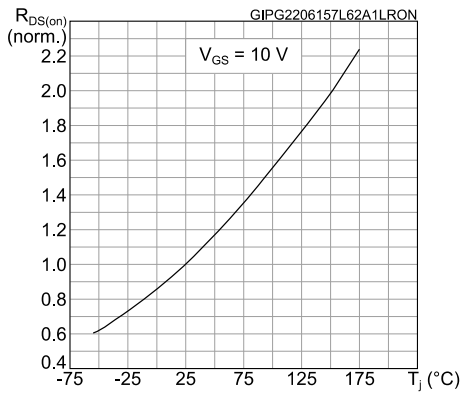


Figure 11: Normalized V(BR)DSS vs temperature

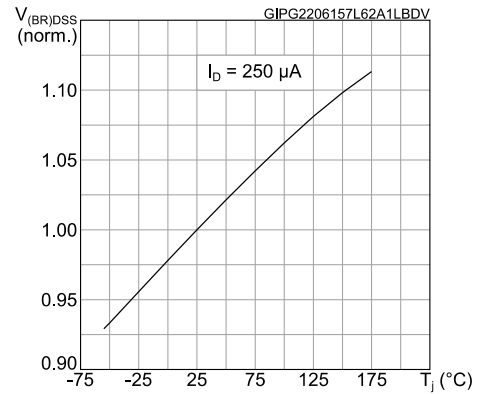
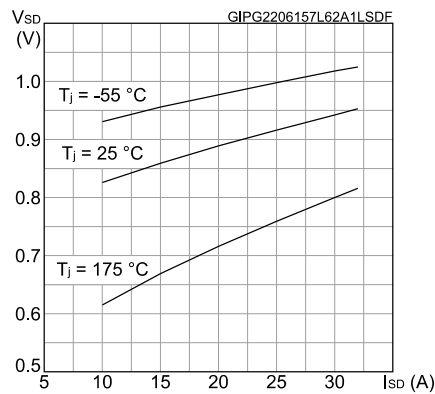
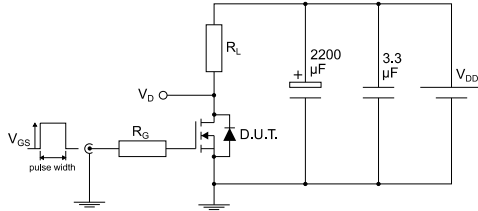


Figure 12: Source-drain diode forward characteristics



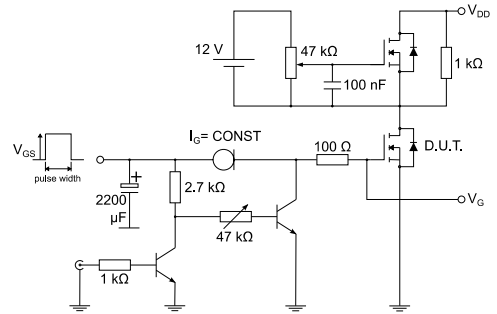
### 3 Test circuits

**Figure 13: Test circuit for resistive load switching times**



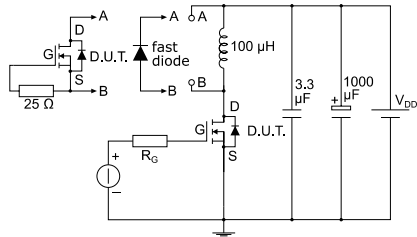
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**Figure 14: Test circuit for gate charge behavior**



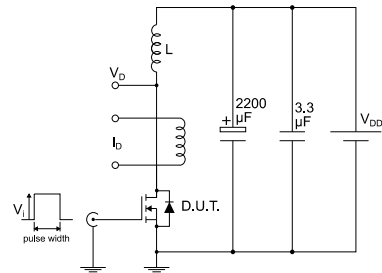
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**Figure 15: Test circuit for inductive load switching and diode recovery times**



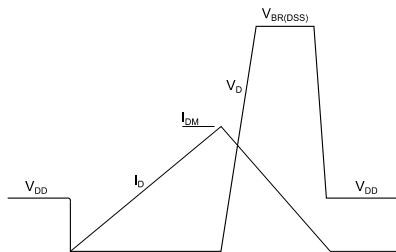
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**Figure 16: Unclamped inductive load test circuit**



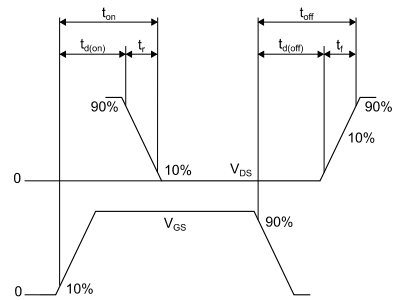
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**Figure 17: Unclamped inductive waveform**



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**Figure 18: Switching time waveform**



AM01473v1



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 4.1 PowerFLAT™ 5x6 double island WF type R package information

Figure 19: PowerFLAT™ 5x6 double island WF type R package outline

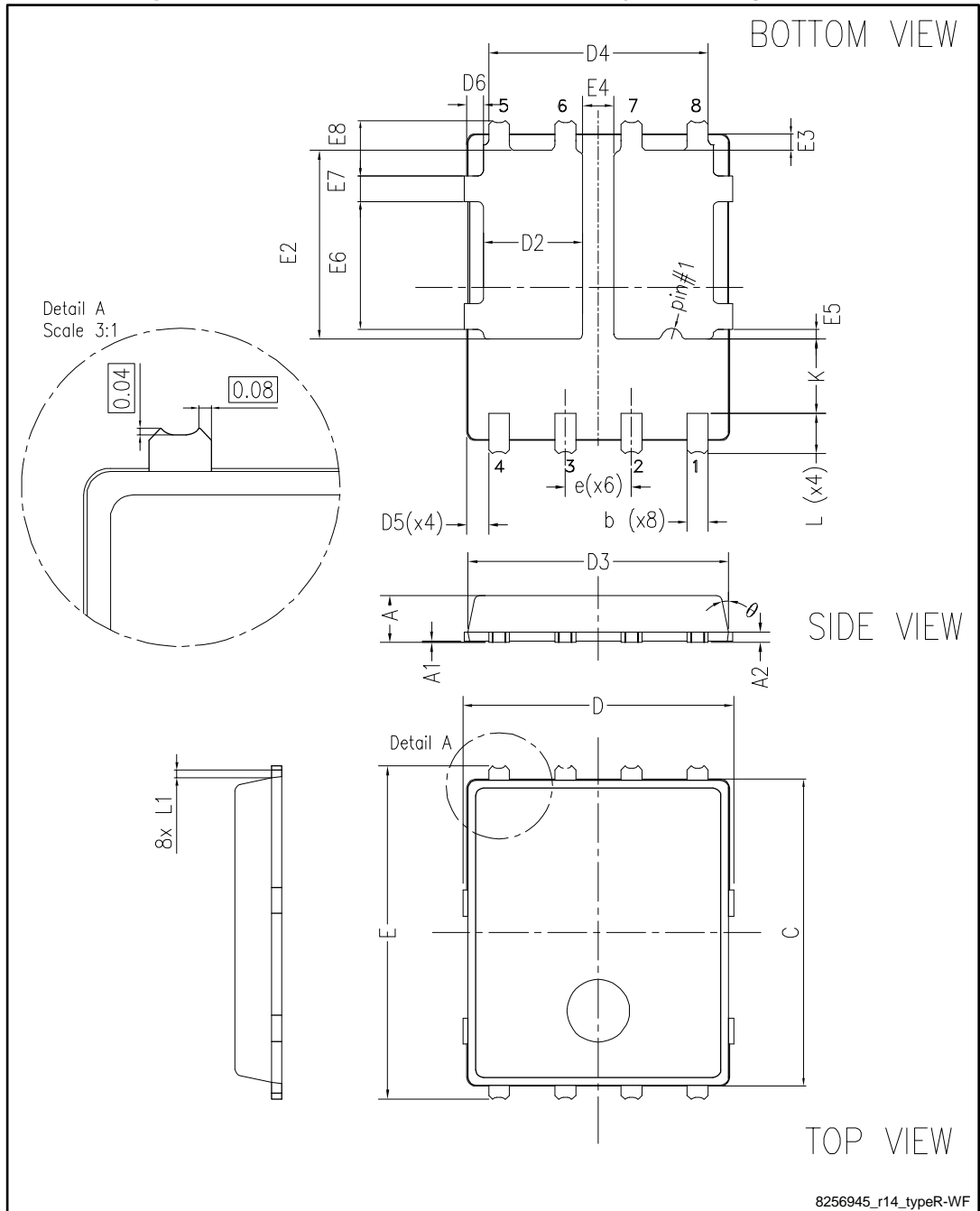


Table 9: PowerFLAT™ 5x6 double island WF type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	1.68		1.88
D3	4.80	5.00	5.20
D4	4.05	4.20	4.35
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	6.20	6.40	6.60
E2	3.50		3.70
E3	0.20	0.325	0.45
E4	0.55		0.75
E5	0.08		0.28
E6	2.35		2.55
E7	0.40		0.60
E8	0.85	1.00	1.15
K	1.275		1.575
L	0.70		0.90
L1		0.275	
θ	0°		12°



## 4.2 PowerFLAT™ 5x6 WF packing information

Figure 21: PowerFLAT™ 5x6 WF tape

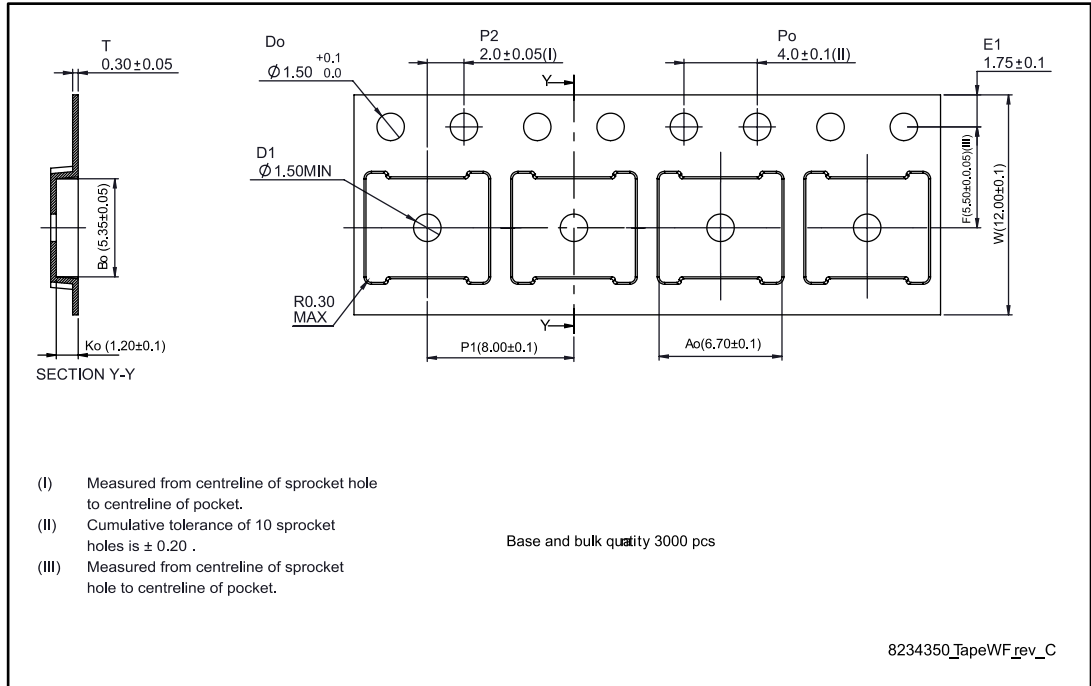


Figure 22: PowerFLAT™ 5x6 package orientation in carrier tape

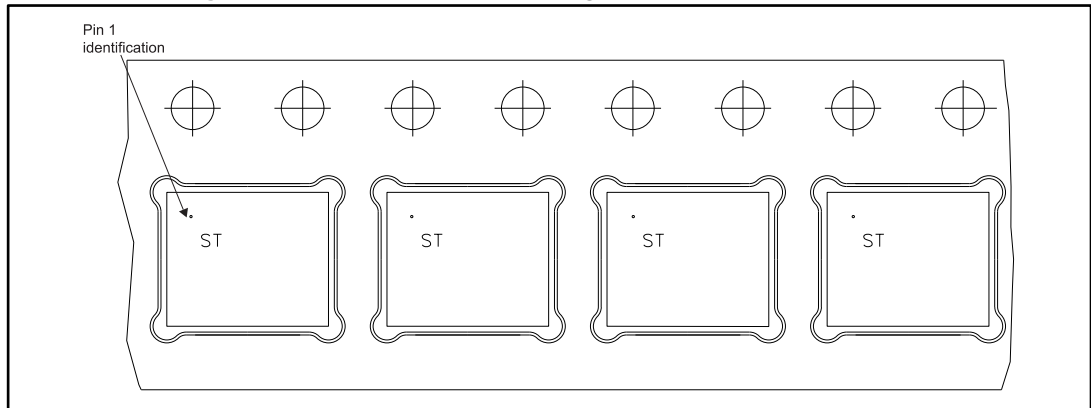
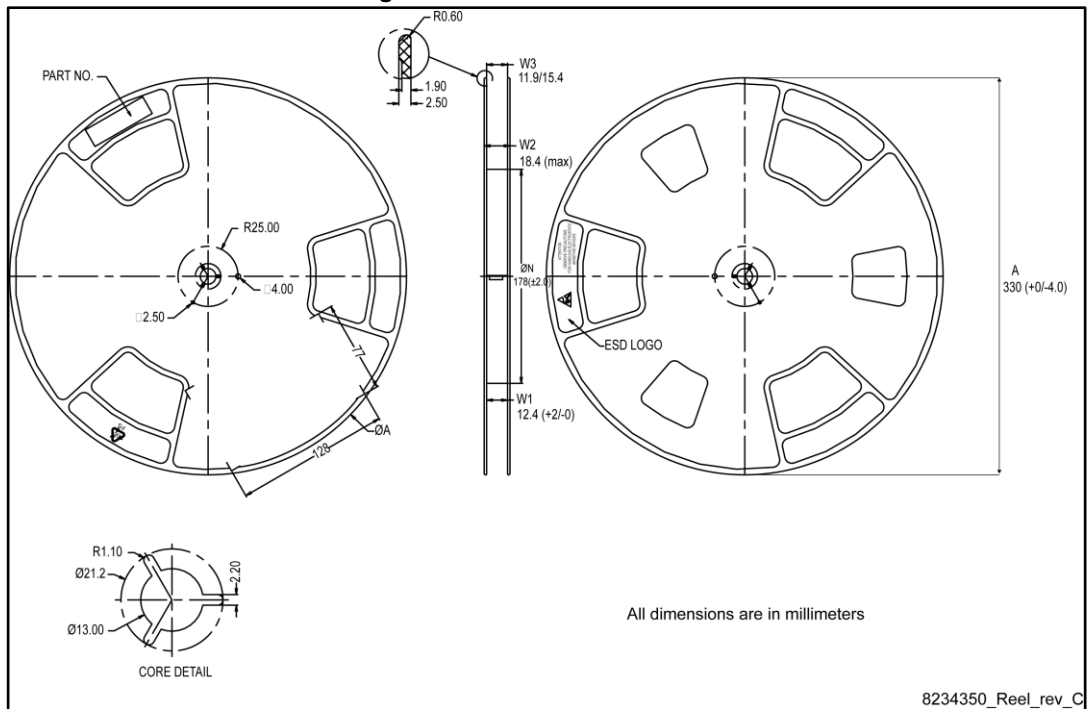


Figure 23: PowerFLAT™ 5x6 reel



## 5 Revision history

Table 10: Document revision history

Date	Revision	Changes
24-Jun-2015	1	First release.
07-Jul-2015	2	Minor text edits throughout document.
20-Jan-2016	3	Updated title. Updated <i>Table 2: "Absolute maximum ratings"</i> , <i>Table 3: "Thermal data"</i> and <i>Table 4: "Avalanche characteristics"</i> . Updated <i>Figure 2: "Safe operating area"</i> and <i>Figure 3: "Thermal impedance"</i> . Minor text changes.

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