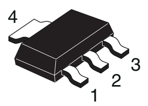
STN3N45K3

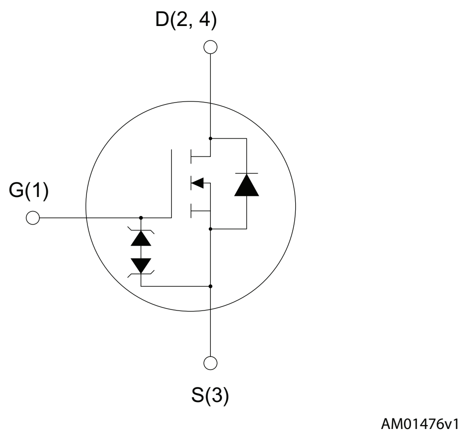
N-channel 450 V - 3.3 Ω typ., 0.6 A Zener-protected, SuperMESH3™ Power MOSFET in a SOT-223 package

Datasheet - production data



SOT-223

Figure 1. Internal schematic diagram



Features

Order code	V_{DSS}	$R_{DS(on)}$ max	I_D	P_w
STN3N45K3	450 V	< 4 Ω	0.6 A	3 W

- 100% avalanche tested
- Extremely high dv/dt capability
- Gate charge minimized
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- Switching applications

Description

This SuperMESH3™ Power MOSFET is the result of improvements applied to STMicroelectronics’ SuperMESH™ technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

Table 1. Device summary

Order code	Marking	Package	Packaging
STN3N45K3	3N45K3	SOT-223	Tape and reel

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	450	V
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at T_{amb} = 25 °C	0.6	A
I_{DM} (1)	Drain current (pulsed)	2.4	A
P_{TOT}	Total dissipation at T_{amb} = 25 °C	3	W
I_{AR} (2)	Avalanche current, repetitive or not-repetitive	0.6	A
E_{AS} (3)	Single pulse avalanche energy (starting T_j = 25°C, I_D = I_{AR}, V_{DD} = 50V)	45	mJ
dv/dt (4)	Peak diode recovery voltage slope	12	V/ns
Vesd(g-s)	G-S ESD (HBM C = 100 pF, R = 1.5 kΩ)	1000	V
T_{stg}	Storage temperature	-55 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area.
2. Pulse width limited by Tj max.
3. Starting Tj = 25 °C, I_D = I_{AR}, V_{DD} = 50 V.
4. I_{SD} ≤ 0.6 A, di/dt ≤ 400 A/µs, V_{DS} peak ≤ $V_{(BR)DSS}$, V_{DD} = 80% $V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thj-a} (1)	Thermal resistance junction-ambient	37.8	°C/W

1. When mounted on FR-4 board of 1 inch^2 , 2oz Cu, t < 30 sec

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS} = 0	450			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = 450 V V_{DS} = 450 V, T_C=125 °C			1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			± 10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 50 µA	3	3.75	4.5	V
$R_{DS(on}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 0.6 A		3.3	4	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 50 V, f = 1 MHz, V_{GS} = 0	-	164	-	pF
C_{oss}	Output capacitance		-	17	-	pF
C_{rss}	Reverse transfer capacitance		-	3	-	pF
$C_{o(tr)}$(1)	Equivalent capacitance time related	V_{DS} = 0 to 360 V, V_{GS} = 0	-	13	-	pF
$C_{o(er)}$(2)	Equivalent capacitance energy related		-	18	-	pF
R_G	Intrinsic gate resistance	f = 1 MHz open drain	-	8	-	Ω
Q_g	Total gate charge	V_{DD} = 360 V, I_D = 1.8 A, V_{GS} = 10 V (see *Figure 16*)	-	9.5	-	nC
Q_{gs}	Gate-source charge		-	2	-	nC
Q_{gd}	Gate-drain charge		-	6	-	nC

1. $C_{oss\ eq.}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. $C_{oss\ eq.}$ energy related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 225 V, I_D = 0.9 A, R_G = 4.7 Ω, V_{GS} = 10 V (see *Figure 15*)	-	6.5	-	ns
t_r	Rise time		-	5.4	-	ns
$t_{d(off)}$	Turn-off-delay time		-	17	-	ns
t_f	Fall time		-	22	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		0.6	A
I_{SDM} (1)	Source-drain current (pulsed)		-		2.4	A
V_{SD} (2)	Forward on voltage	I_{SD} = 0.6 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 1.8 A, di/dt = 100 A/µs V_{DD} = 60 V (see *Figure 20*)	-	175		ns
Q_{rr}	Reverse recovery charge		-	550		nC
I_{RRM}	Reverse recovery current		-	6		A
t_{rr}	Reverse recovery time	I_{SD} = 1.8 A, di/dt = 100 A/µs V_{DD} = 60 V, T_j = 150 °C (see *Figure 20*)	-	185		ns
Q_{rr}	Reverse recovery charge		-	600		nC
I_{RRM}	Reverse recovery current		-	6.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5%.

Table 8. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	I_{GS}= ± 1 mA, I_D=0	30	-	-	V

The built-in back-to-back Zener diodes have been specifically designed to enhance not only the device's ESD capability, but also to make them capable of safely absorbing any voltage transients that may occasionally be applied from gate to source. In this respect, the Zener voltage is appropriate to achieve efficient and cost-effective protection of device integrity. The integrated Zener diodes thus eliminate the need for external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

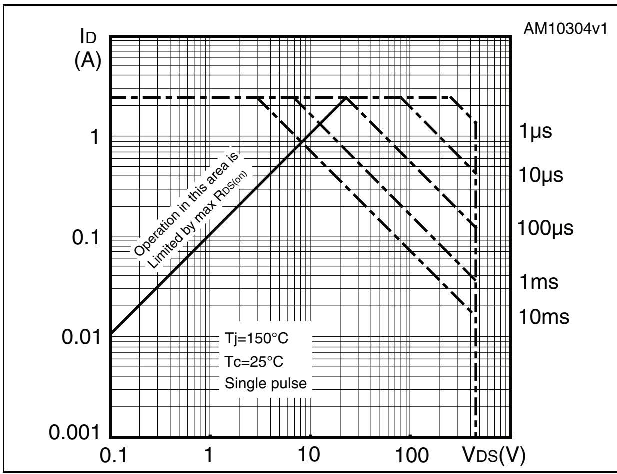


Figure 3. Thermal impedance

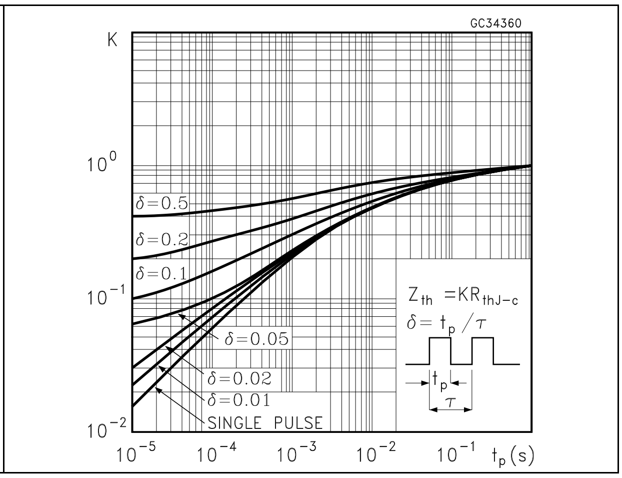


Figure 4. Output characteristics

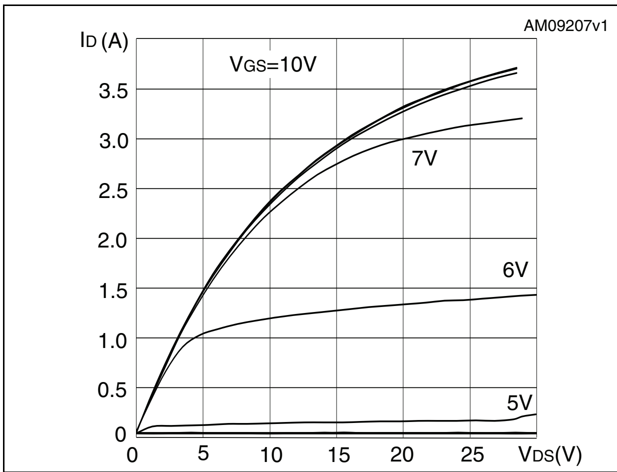


Figure 5. Transfer characteristics

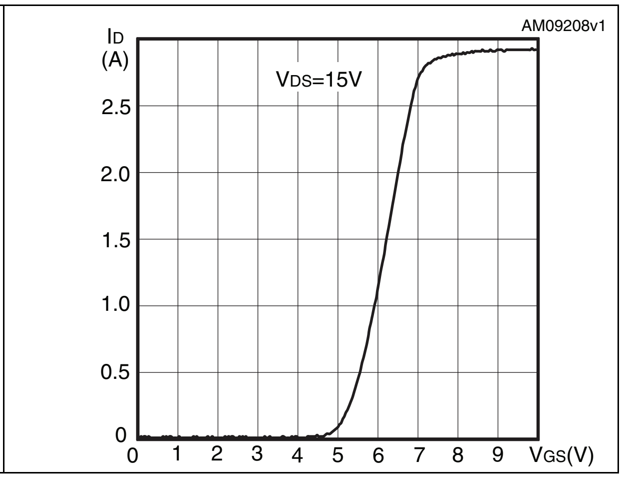


Figure 6. Gate charge vs gate-source voltage

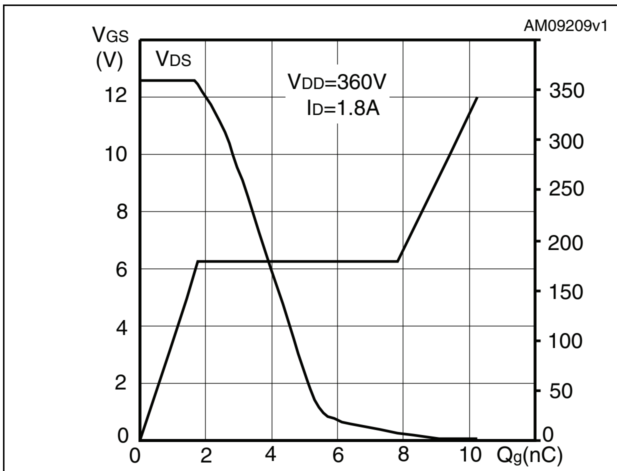


Figure 7. Static drain-source on resistance

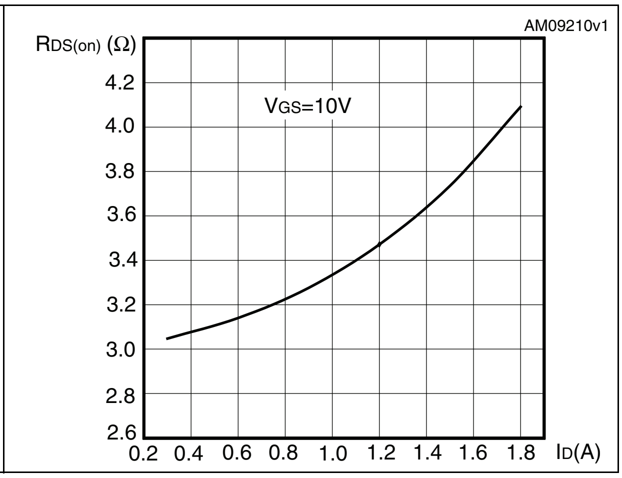


Figure 8. Capacitance variations

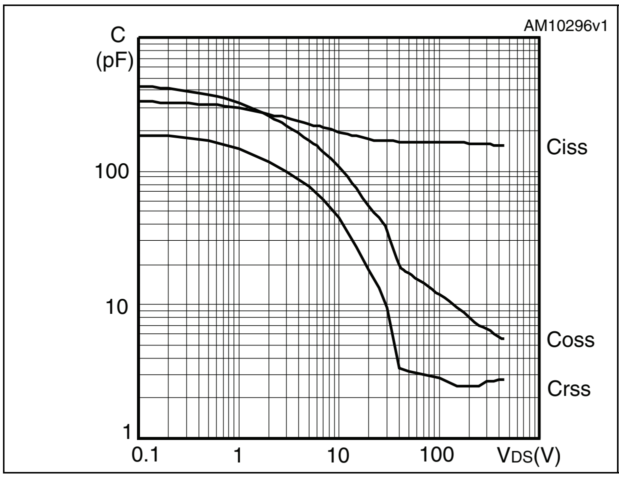


Figure 9. Output capacitance stored energy

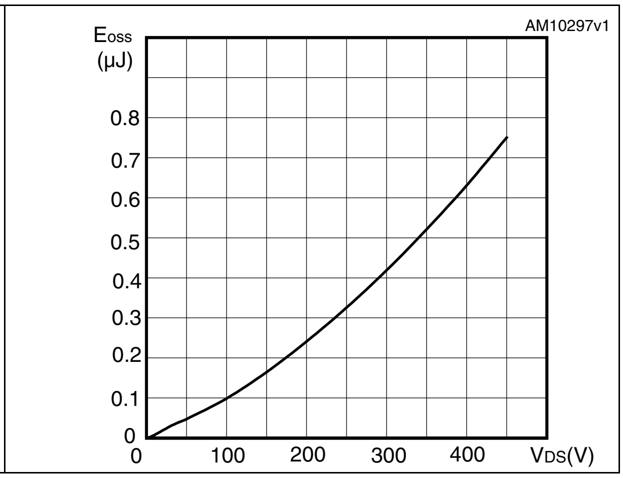


Figure 10. Normalized gate threshold voltage vs temperature

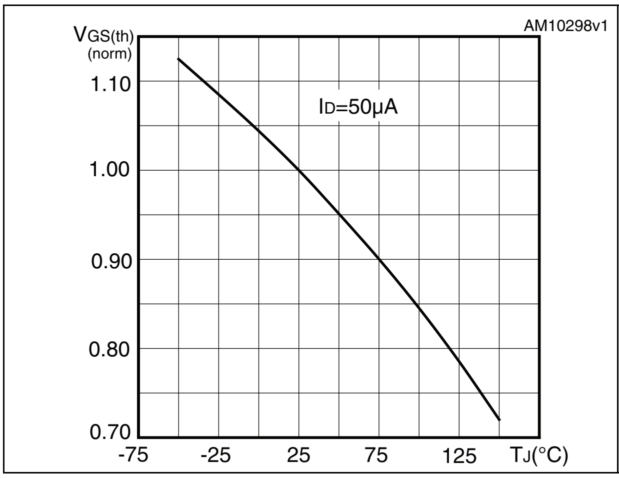


Figure 11. Normalized on-resistance vs temperature

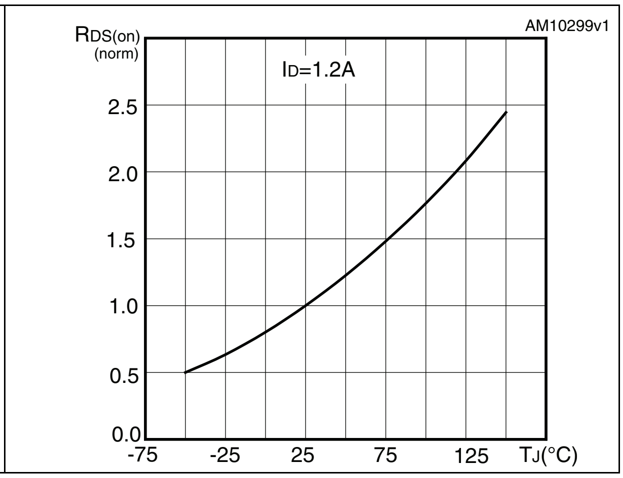


Figure 12. Source-drain diode forward characteristics

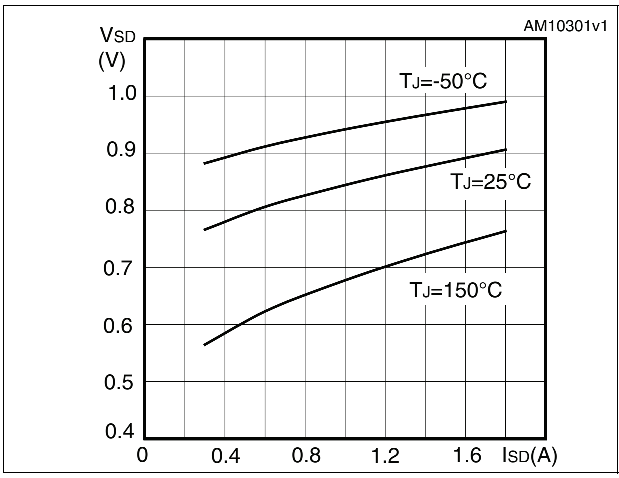


Figure 13. Normalized B_{VDSS} vs temperature

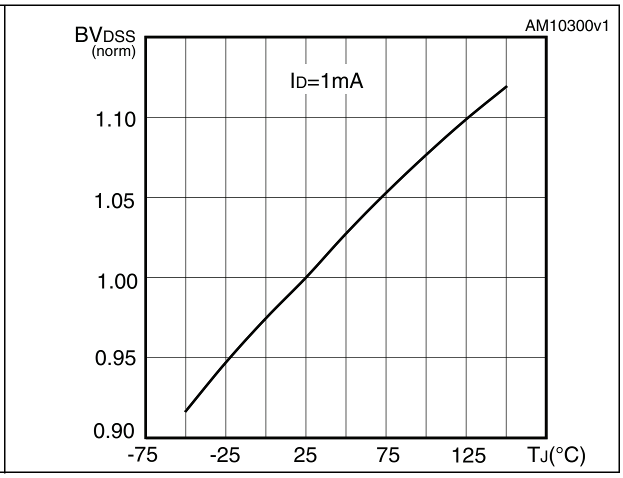
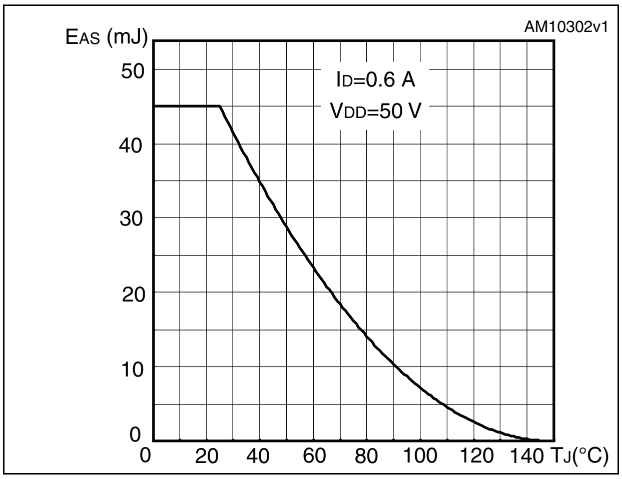


Figure 14. Maximum avalanche energy vs starting Tj



3 Test circuits

Figure 15. Switching times test circuit for resistive load

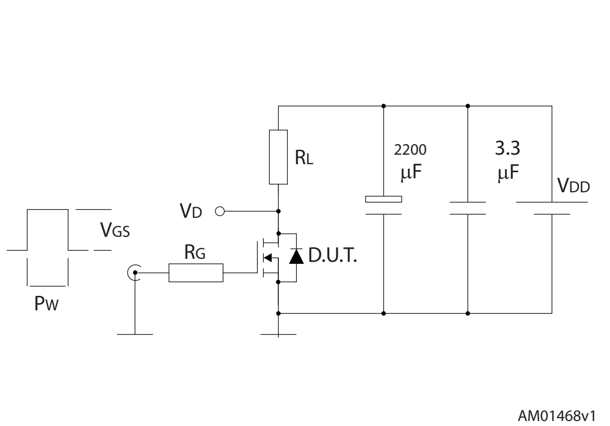


Figure 16. Gate charge test circuit

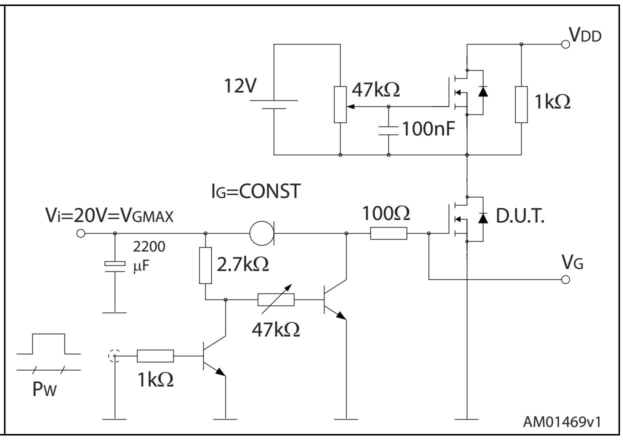


Figure 17. Test circuit for inductive load switching and diode recovery times

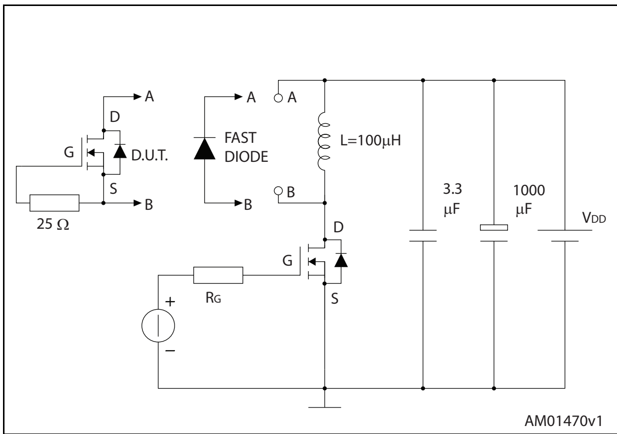


Figure 18. Unclamped inductive load test circuit

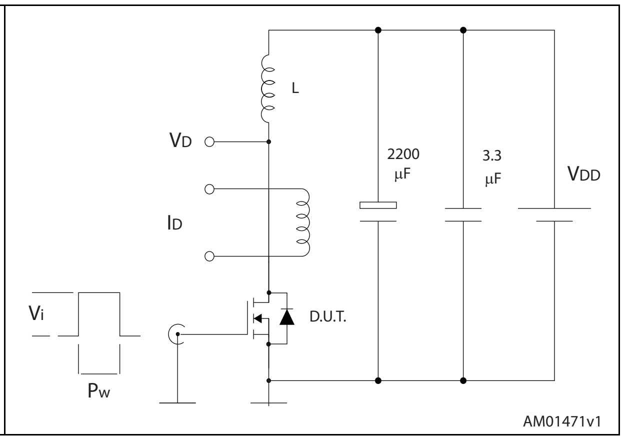


Figure 19. Unclamped inductive waveform

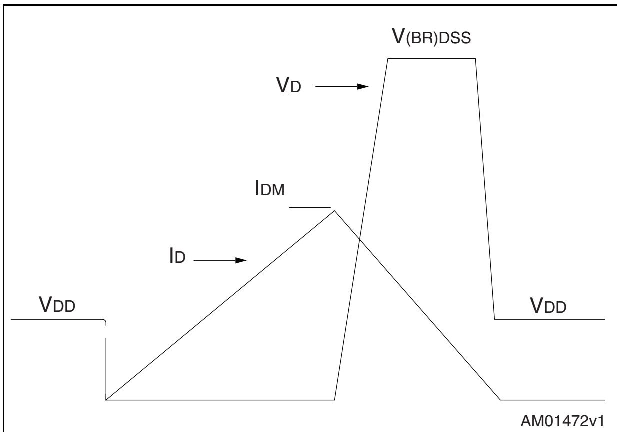
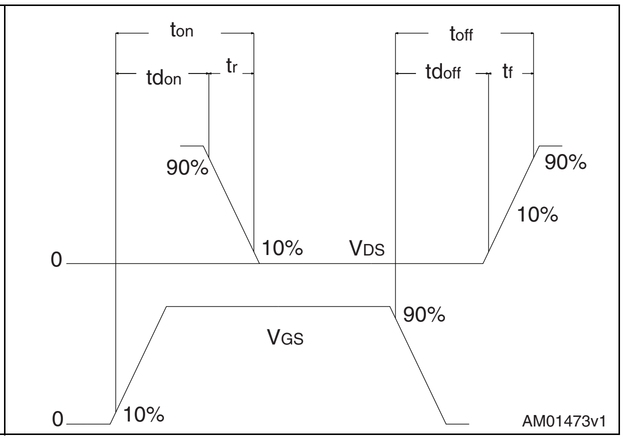


Figure 20. Switching time waveform



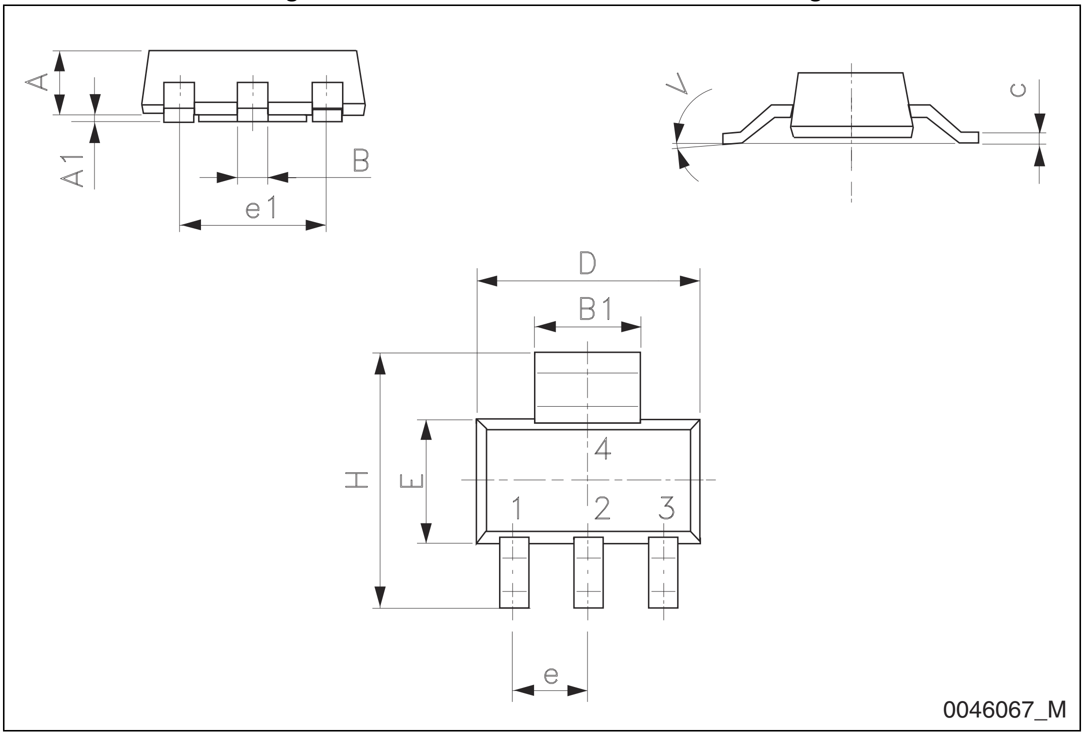
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 9. SOT-223 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.80
A1	0.02		0.1
B	0.60	0.70	0.85
B1	2.90	3.00	3.15
c	0.24	0.26	0.35
D	6.30	6.50	6.70
e		2.30	
e1		4.60	
E	3.30	3.50	3.70
H	6.70	7.00	7.30
V			10°

Figure 21. SOT-223 mechanical data drawing

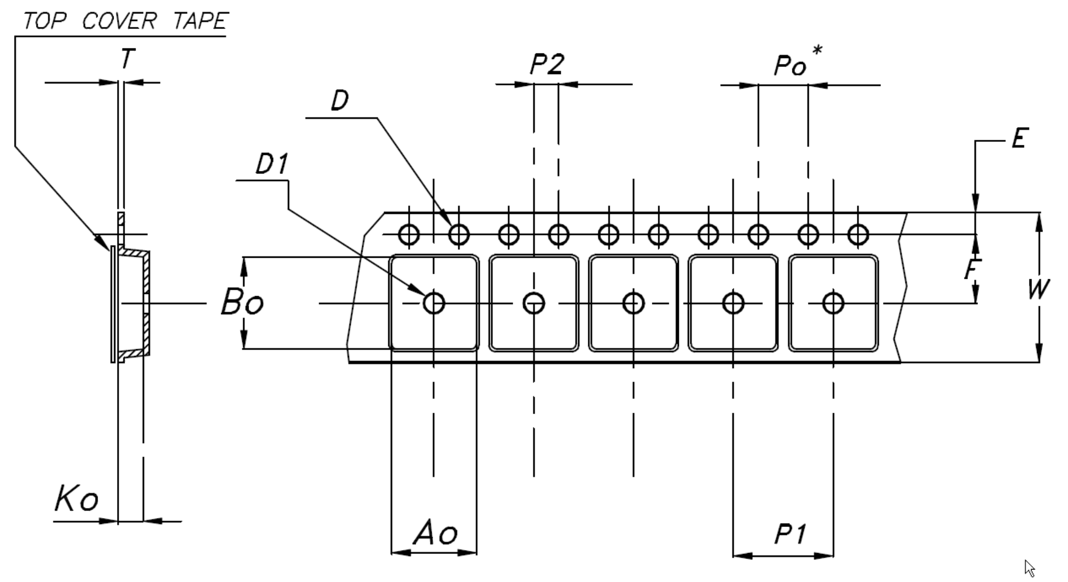


5 Packaging mechanical data

Table 10. SOT-223 tape and reel mechanical data

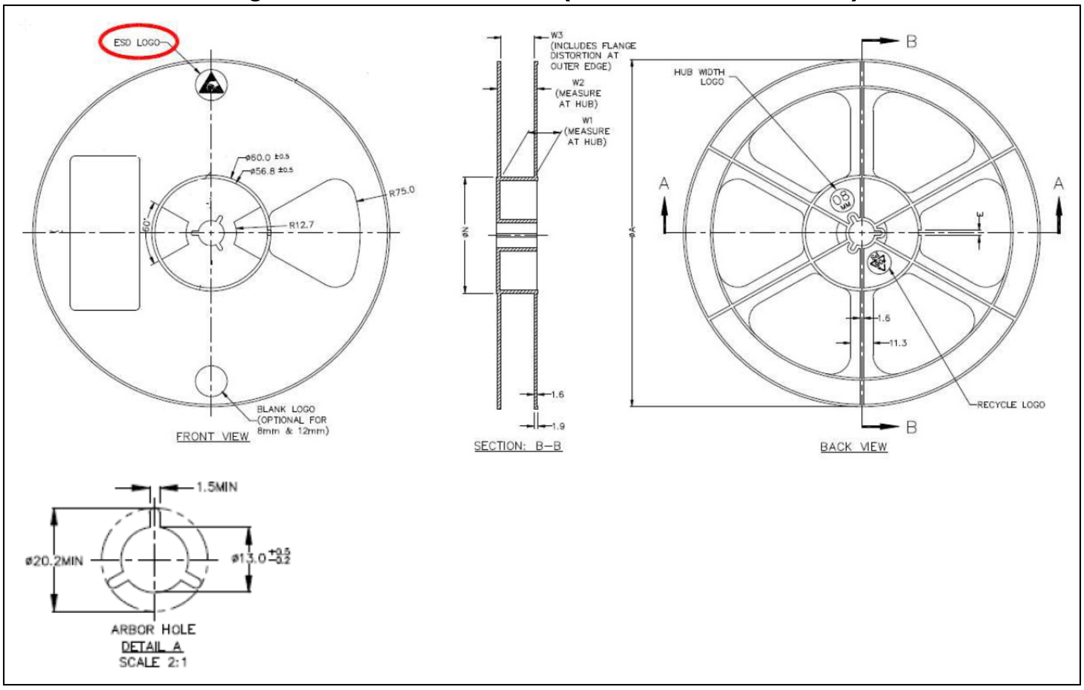
Tape				Reel		
Dim.	mm			Dim.	mm	
	Min.	Typ.	Max.		Min.	Max.
A0	6.75	6.85	6.95	A		180
B0	7.30	7.40	7.50	N	60	
K0	1.80	1.90	2.00	W1		12.4
F	5.40	5.50	5.60	W2		18.4
E	1.65	1.75	1.85	W3	11.9	15.4
W	11.7	12	12.3			
P2	1.90	2	2.10	Base quantity pcs		1000
P0	3.90	4	4.10	Bulk quantity pcs		1000
P1	7.90	8	8.10			
T	0.25	0.30	0.35			
Dϕ	1.50	1.55	1.60			
D1ϕ	1.50	1.60	1.70			

Figure 22. Tape for SOT-223 (dimensions are in mm)



*Cumulative tolerance of 10 sprocket holes is ±0.20 mm

Figure 23. Reel for TO-223 (dimensions are in mm)



6 Revision history

Table 11. Document revision history

Date	Revision	Changes
25-Jun-2013	1	First release. Part number previously included in datasheet DocID17206