

## P-channel 30 V, 0.16 $\Omega$ typ., 7 A, STripFET™ II Power MOSFET in a SO-8 package

Datasheet - production data

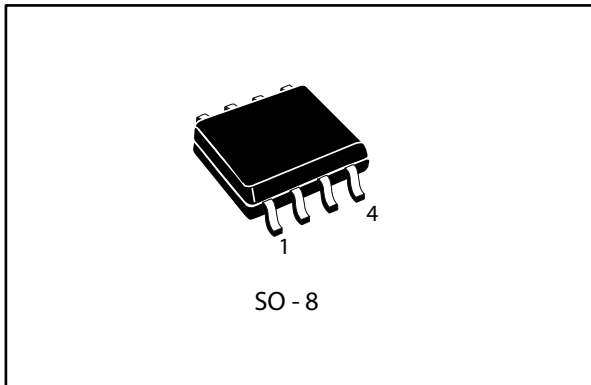


Figure 1: Internal schematic diagram

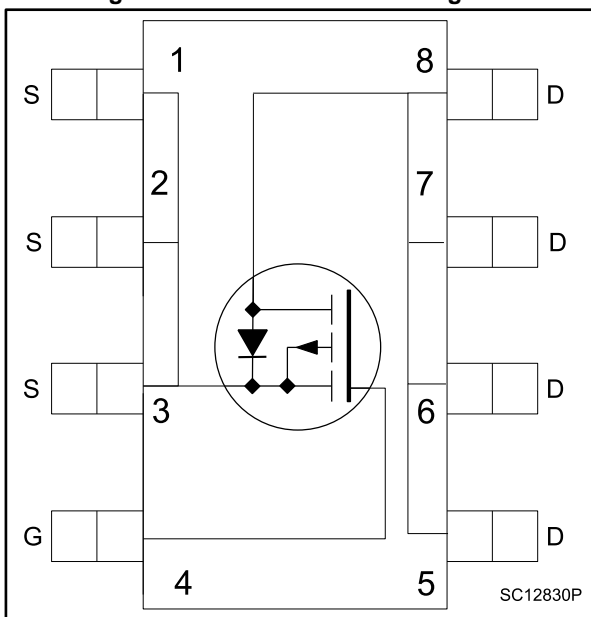


Table 1: Device summary

Order code	Marking	Package	Packaging
STS7PF30L	7PF30L	SO-8	Tape and reel

### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STS7PF30L	30 V	0.021 $\Omega$	7 A

- Standard outline for easy automated surface mount assembly
- Low threshold drive

### Applications

- Switching applications

### Description

This Power MOSFET series realized with STMicroelectronics unique STripFET™ process is specifically designed to minimize input capacitance and gate charge. It is therefore ideal as a primary switch in advanced high-efficiency isolated DC-DC converters for Telecom and Computer applications. It is also suitable for any application with low gate charge drive requirements.

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# 1 Electrical ratings

**Table 2: Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	30	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$V_{DGR}$	Drain-gate voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	30	V
$I_D$	Drain current (continuous) at $T_{amb} = 25 \text{ }^\circ\text{C}$	7	A
$I_D$	Drain current (continuous) at $T_{amb} = 100 \text{ }^\circ\text{C}$	4.4	A
$I_{DM}^{(1)}$	Drain current (pulsed)	28	A
$P_{TOT}$	Total dissipation at $T_{amb} = 25 \text{ }^\circ\text{C}$	2.5	W
$T_{stg}$	Storage temperature range	-55 to 150	$^\circ\text{C}$
$T_j$	Operating junction temperature range		$^\circ\text{C}$

**Notes:**

<sup>(1)</sup>Pulse width limited by safe operating area.

**Table 3: Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-amb}^{(1)}$	Thermal resistance junction-amb	50	$^\circ\text{C/W}$

**Notes:**

<sup>(1)</sup>When mounted on 1 inch<sup>2</sup> FR-4 board, 2 oz. Cu.,  $t \leq 10 \text{ s}$



For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4: Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	30			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 30\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 30\text{ V}$ , $T_C = 125\text{ °C}$ <sup>(1)</sup>			10	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 16\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1	1.6	2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 3.5\text{ A}$	0.011	0.016	0.021	$\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 3.5\text{ A}$	0.016	0.022	0.028	

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production test.

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}$	Forward transconductance	$V_{DS} = 20\text{ V}$ , $I_D = 3.5\text{ A}$	-	16		S
$C_{ISS}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	2600		pF
$C_{OSS}$	Output capacitance		-	523		pF
$C_{RSS}$	Reverse transfer capacitance		-	174		pF
$Q_g$	Total gate charge	$V_{DD} = 15\text{ V}$ , $I_D = 7\text{ A}$ , $V_{GS} = 4.5\text{ V}$ (see <a href="#">Figure 15: "Gate charge test circuit"</a> )	-	28	38	nC
$Q_{gs}$	Gate-source charge		-	8.75		nC
$Q_{gd}$	Gate-drain charge		-	12.35		nC

**Table 6: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}$ , $I_D = 3.5\text{ A}$ $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 4.5\text{ V}$ (see <a href="#">Figure 14: "Switching times test circuit for resistive load"</a> )	-	68	-	ns
$t_r$	Rise time		-	54	-	ns
$t_{d(off)}$	Turn-off-delay time		-	65	-	ns
$t_f$	Fall time		-	23	-	ns



For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		7	A
$I_{SDM}$	Source-drain current (pulsed)		-		28	A
$V_{SD}^{(1)}$	Forward on voltage	$V_{GS} = 0 \text{ V}$ , $I_{SD} = 7 \text{ A}$	-		1.2	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 7 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 15 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 16: "Test circuit for inductive load switching and diode recovery times"</a> )	-	40		ns
$Q_{rr}$	Reverse recovery charge		-	46		nC
$I_{RRM}$	Reverse recovery current		-	2.3		A

**Notes:**

<sup>(1)</sup> Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%



For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.

## 2.2 Electrical characteristics (curves)

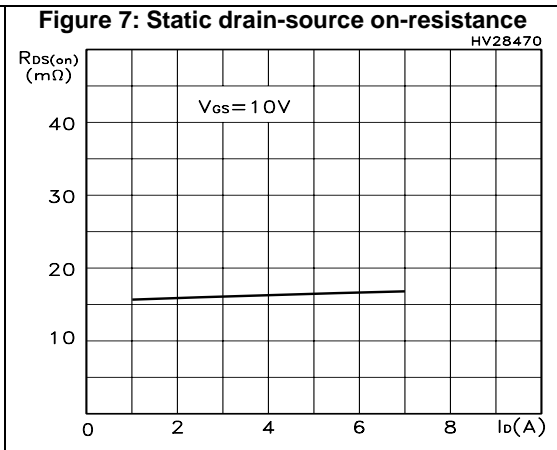
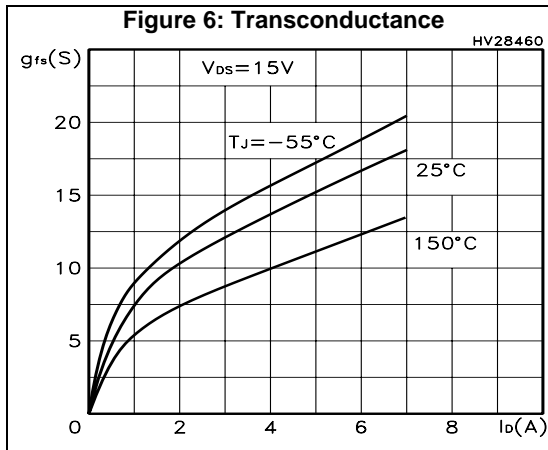
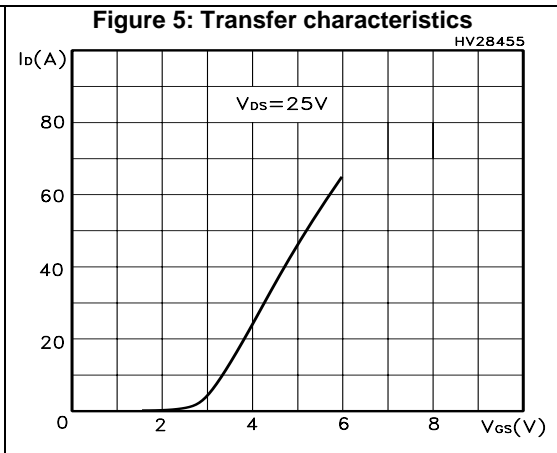
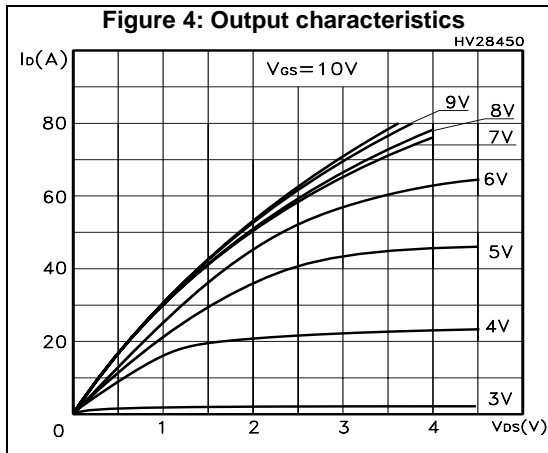
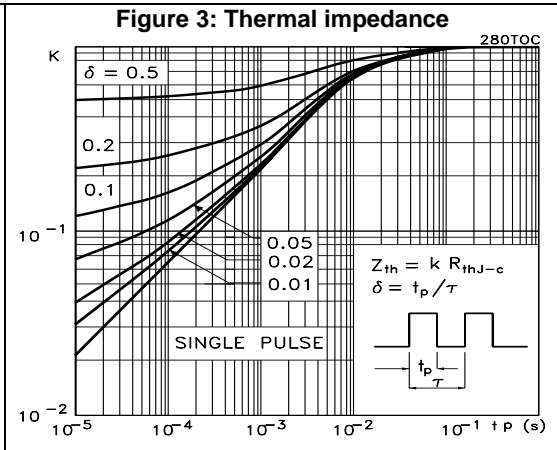
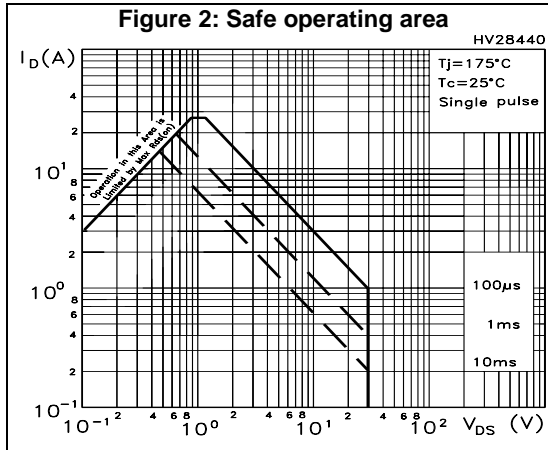


Figure 8: Gate charge vs gate-source voltage

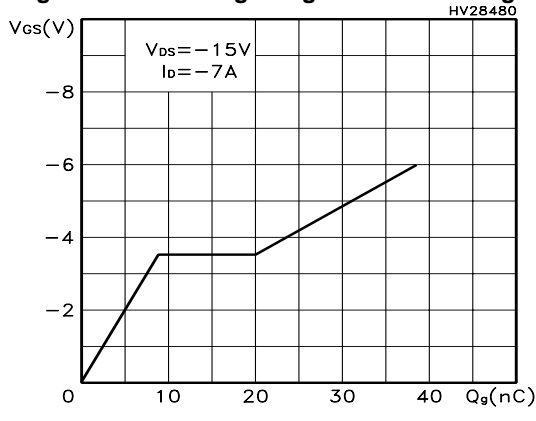


Figure 9: Capacitance variations

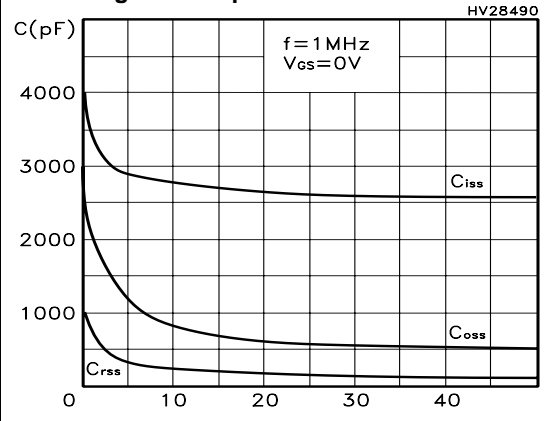


Figure 10: Normalized gate threshold voltage vs temperature

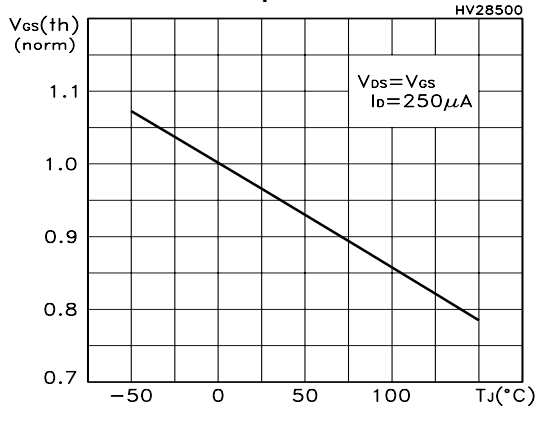


Figure 11: Normalized on-resistance vs temperature

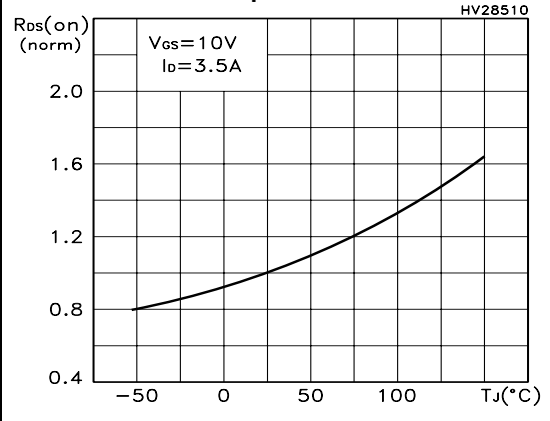


Figure 12: Source-drain diode forward characteristics

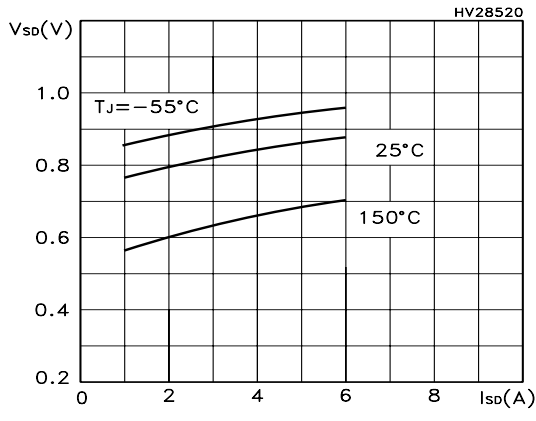
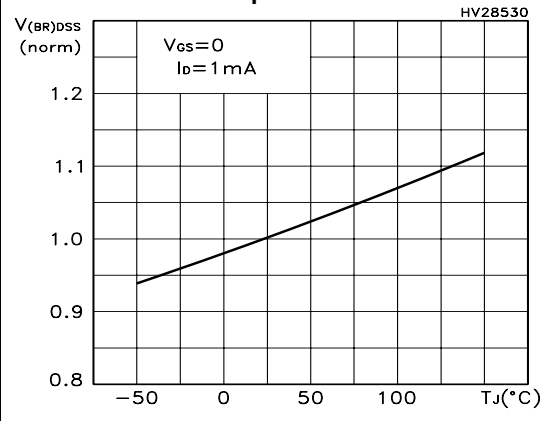
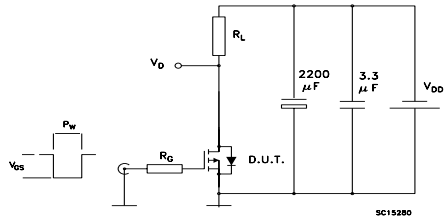


Figure 13: Normalized breakdown voltage vs temperature

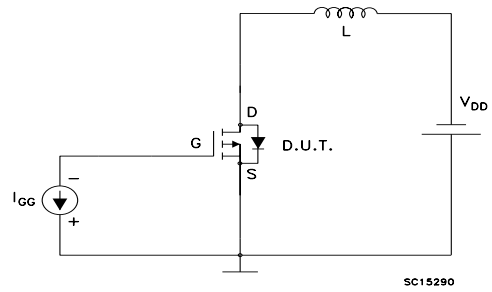


### 3 Test circuits

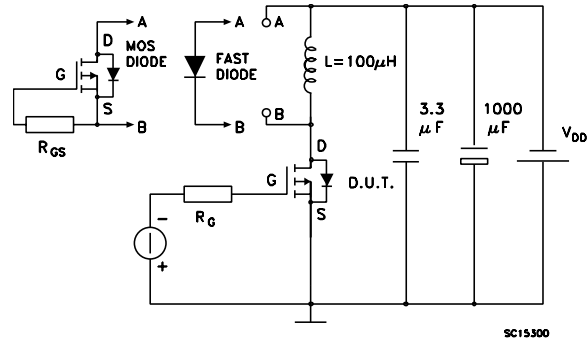
**Figure 14: Switching times test circuit for resistive load**



**Figure 15: Gate charge test circuit**



**Figure 16: Test circuit for inductive load switching and diode recovery times**





## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 SO-8 package information

Figure 17: SO-8 package outline

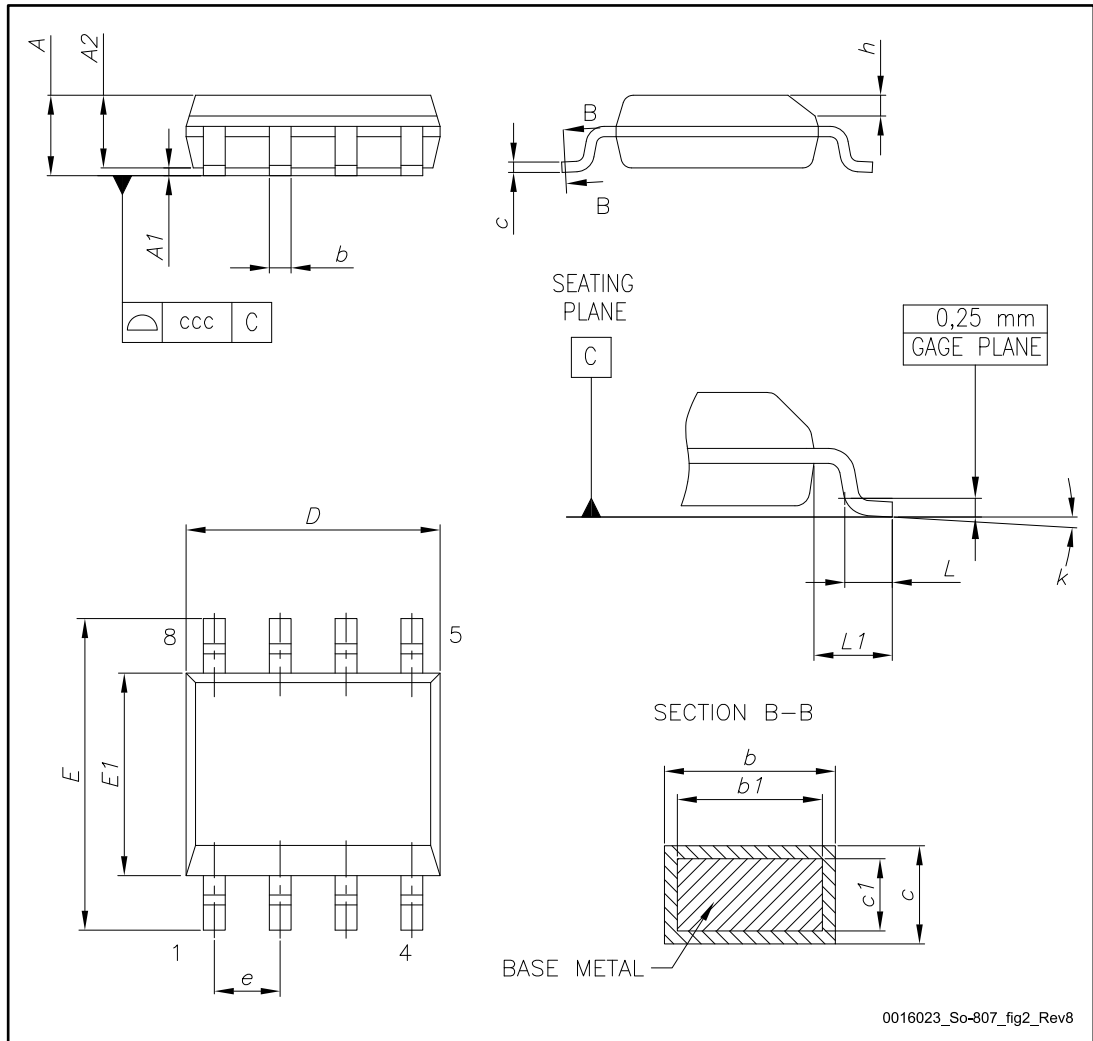
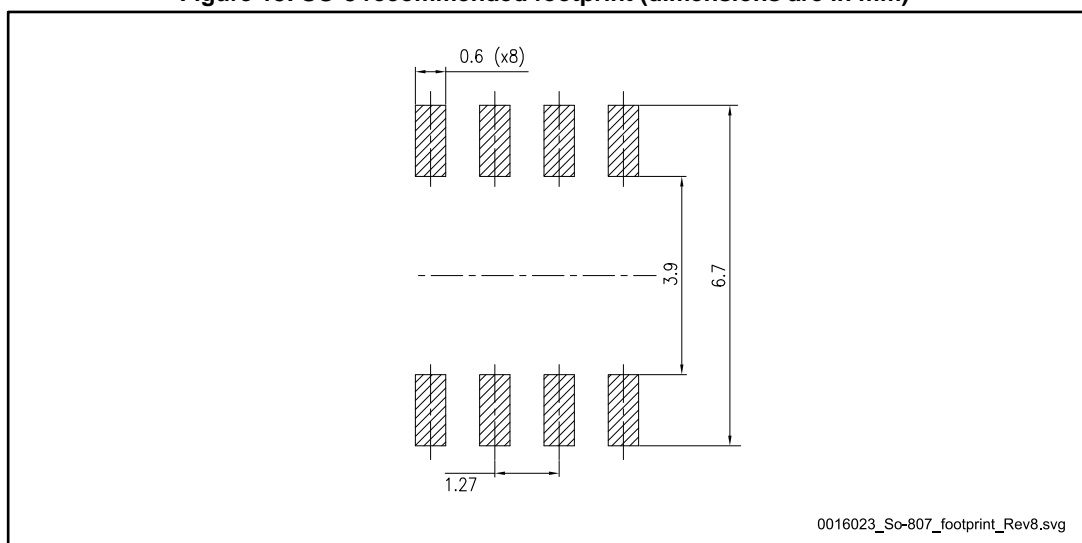


Table 8: SO-8 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.31		0.51
b1	0.28		0.48
c	0.10		0.25
c1	0.10		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
L2		0.25	
k	0°		8°
ccc			0.10

Figure 18: SO-8 recommended footprint (dimensions are in mm)



## 4.2 Packing information

Figure 19: SO-8 tape and reel dimensions

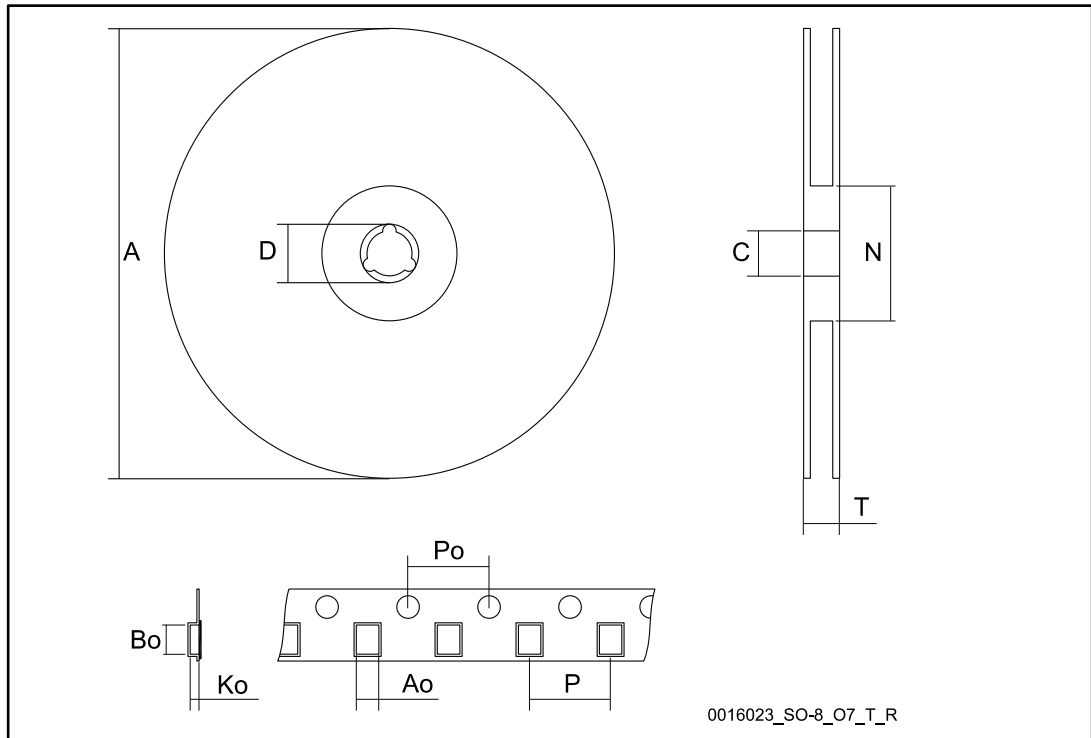


Table 9: SO-8 tape and reel mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			330
C	12.8		13.2
D	20.2		
N	60		
T			22.4
Ao	8.1		8.5
Bo	5.5		5.9
Ko	2.1		2.3
Po	3.9		4.1
P	7.9		8.1

## 5 Revision history

Table 10: Document revision history

Date	Revision	Changes
13-Dec-2003	1	First revision.
25-Jun-2004	2	Preliminary data.
18-Jan-2005	3	Modified value on Table 6.
29-Sep-2005	4	Complete version.
09-nov-2005	5	The document has been reformatted.
22-Feb-2016	6	Modified: <a href="#">Table 1: "Device summary"</a> in cover page Modified: <a href="#">Table 4: "Static"</a> Minor text changes

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