



# STW20NK50Z

N-channel 500 V, 0.23  $\Omega$ , 20 A SuperMESH™ Power MOSFET  
Zener-protected in TO-247 package

Datasheet — production data

## Features

Order code	V <sub>DSS</sub>	R <sub>DS(on) max</sub>	I <sub>D</sub>	P <sub>W</sub>
STW20NK50Z	500 V	< 0.27 $\Omega$	20 A	190 W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance

## Application

Switching applications

## Description

This device is an N-channel Zener-protected Power MOSFET developed using STMicroelectronics' SuperMESH™ technology, achieved through optimization of ST's well established strip-based PowerMESH™ layout. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.

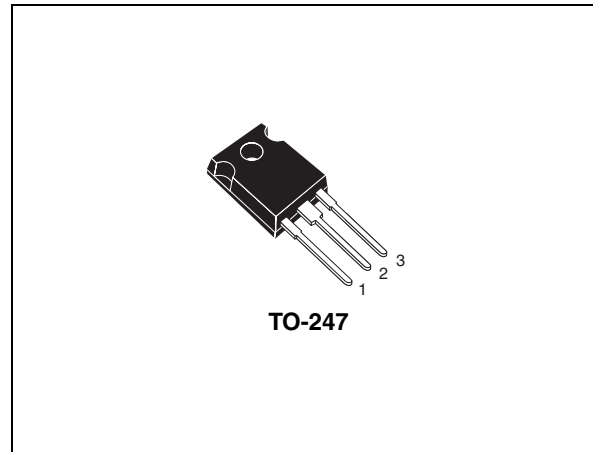


Figure 1. Internal schematic diagram

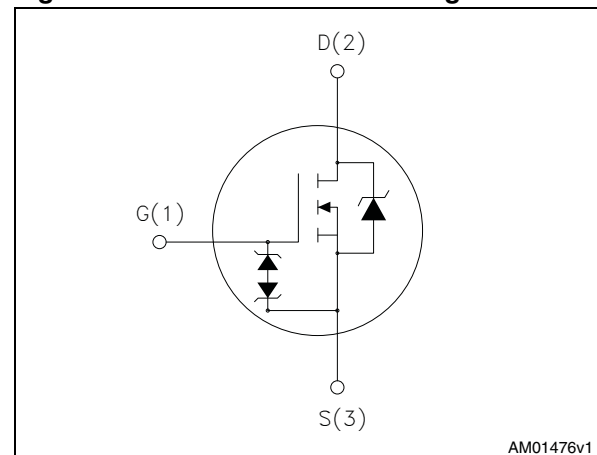


Table 1. Device summary

Order code	Marking	Package	Packaging
STW20NK50Z	W20NK50Z	TO-247	Tube

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	500	V
$V_{GS}$	Gate-source voltage	$\pm 30$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	20	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	12.6	A
$I_{DM}^{(1)}$	Drain current (pulsed)	68	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	190	W
	Derating factor	1.52	W/ $^\circ\text{C}$
ESD	Gate-source human body model ( $R=1.5\text{ k}\Omega$ , $C=100\text{ pF}$ )	6	kV
$dv/dt^{(2)}$	Peak diode recovery voltage slope	4.5	V/ns
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$
$T_j$	Max operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area.

2.  $I_{SD} \leq 17\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DS\text{ peak}} \leq V_{(BR)DSS}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_j \leq T_{JMAX}$ .

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.66	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	$^\circ\text{C}/\text{W}$

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ Max)	17	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j=25\text{ }^\circ\text{C}$ , $I_D=I_{AR}$ , $V_{DD}=50\text{ V}$ )	850	mJ

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	500			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 500\text{ V}$ $V_{DS} = 500\text{ V}$ , $T_C = 125\text{ °C}$			1 50	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 100\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$ , $I_D = 8.5\text{ A}$		0.23	0.27	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$C_{ISS}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$		2600		pF	
$C_{OSS}$	Output capacitance		-	328		pF	
$C_{RSS}$	Reverse transfer capacitance				72	pF	
$C_{OSS\text{ eq.}}$ (1)	Equivalent output capacitance	$V_{DS} = 0$ , $V_{DS} = 0\text{ to }640\text{ V}$	-	187		pF	
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}$ , $I_D = 8.5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 14</a> )		28		ns	
$t_r$	Rise time		-	20		ns	
$t_{d(off)}$	Turn-off delay time				70		ns
$t_f$	Fall time				15		ns
$Q_g$	Total gate charge	$V_{DD} = 400\text{ V}$ , $I_D = 17\text{ A}$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 15</a> )		85	119	nC	
$Q_{gs}$	Gate-source charge		-	15.5		nC	
$Q_{gd}$	Gate-drain charge			42		nC	

1.  $C_{OSS\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{OSS}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$ .

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		20	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		68	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 17\text{ A}$ , $V_{GS} = 0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 17\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_R = 100\text{ V}$ (see <a href="#">Figure 16</a> )	-	355		ns
$Q_{rr}$	Reverse recovery charge			3.90		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			22		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 17\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_R = 100\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 16</a> )	-	440		ns
$Q_{rr}$	Reverse recovery charge			5.72		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			26		A

1. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

2. Pulse width limited by safe operating area.

**Table 8. Gate-source Zener diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$BV_{GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1\text{ mA}$ (open drain)	30	-		V

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

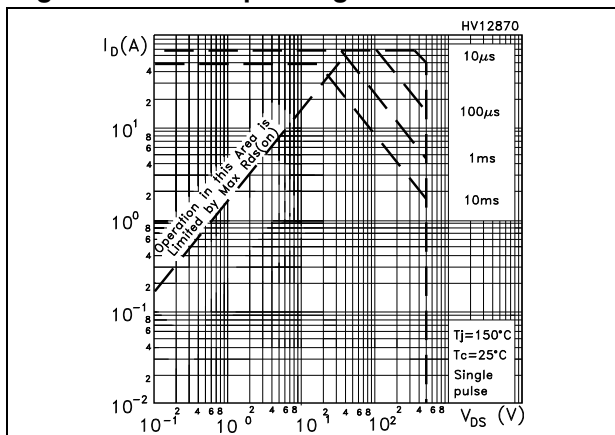


Figure 3. Thermal impedance

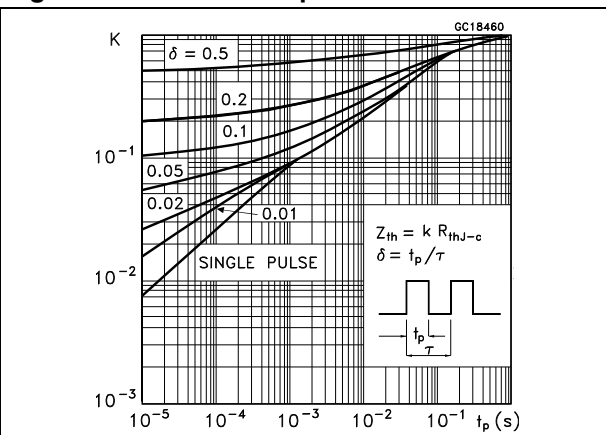


Figure 4. Output characteristics

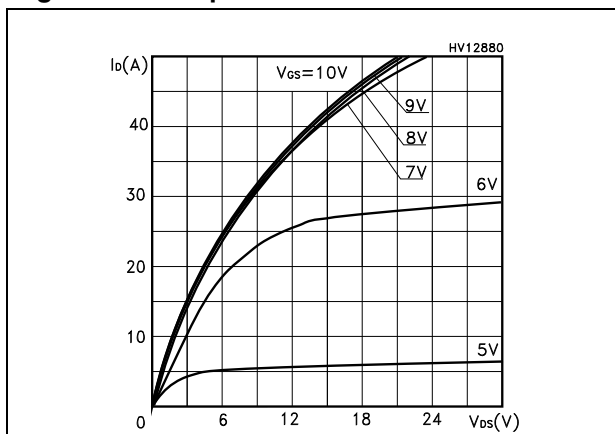


Figure 5. Transfer characteristics

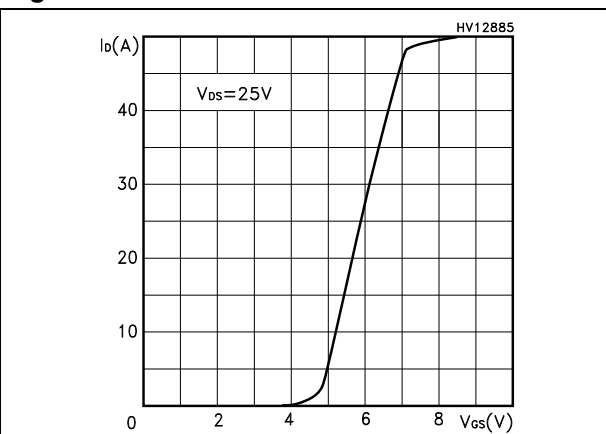


Figure 6. Normalized  $B_{V_{DSS}}$  vs temperature

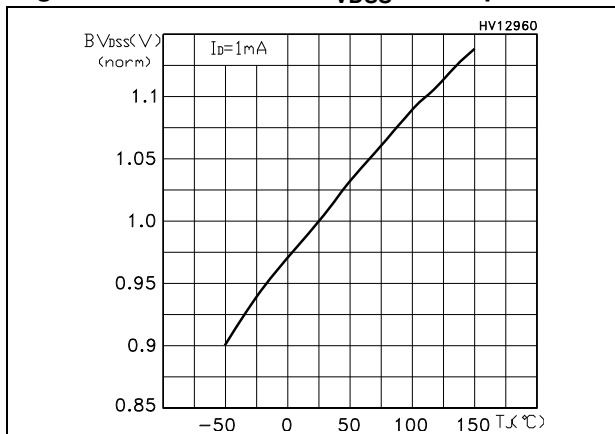


Figure 7. Static drain-source on-resistance

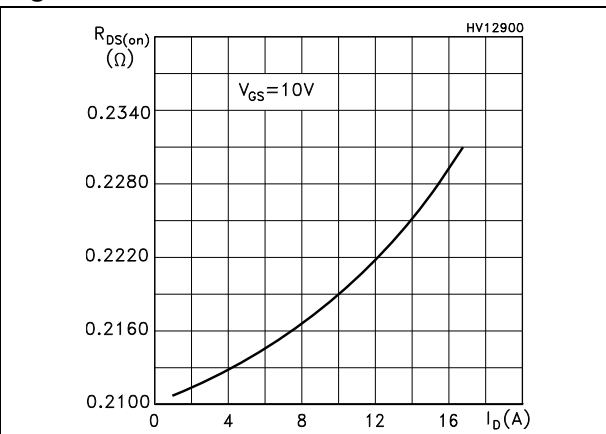


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

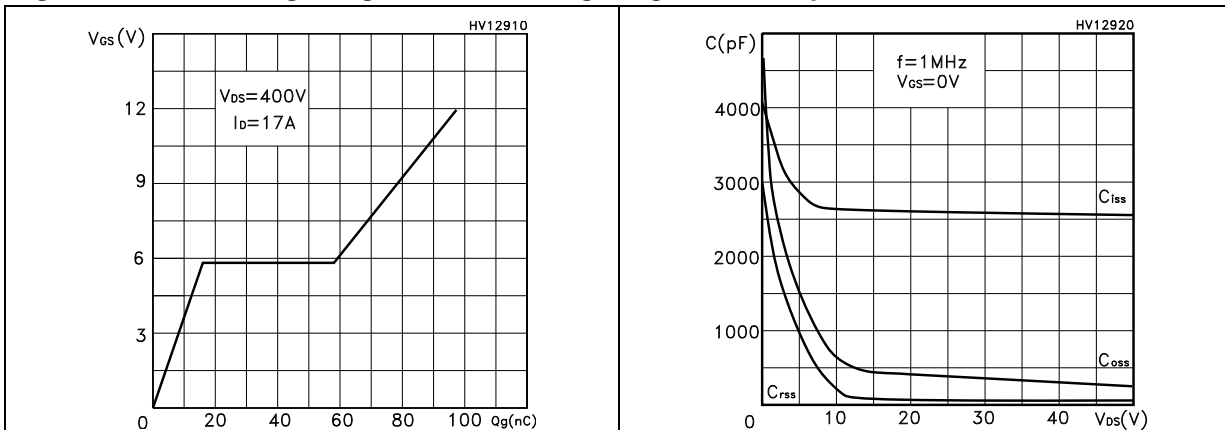


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on-resistance vs temperature

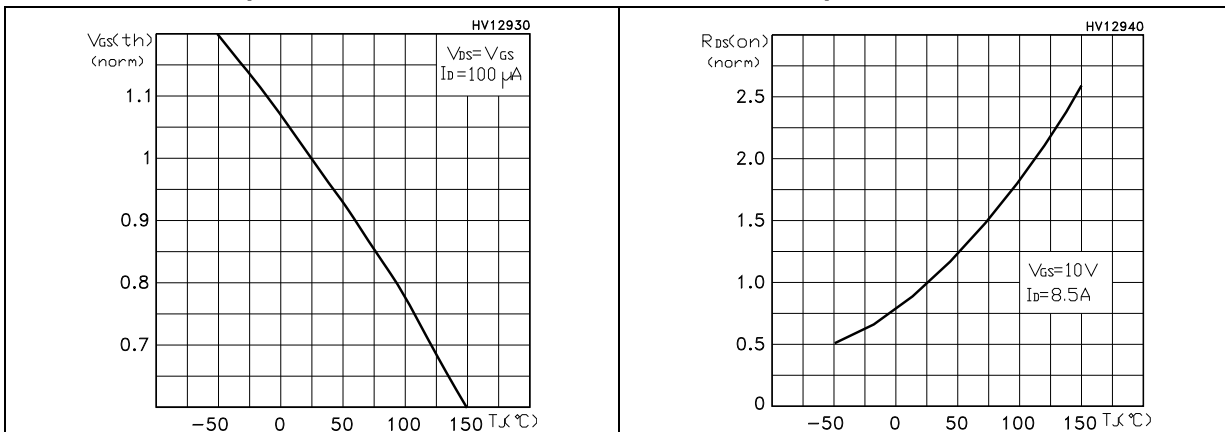
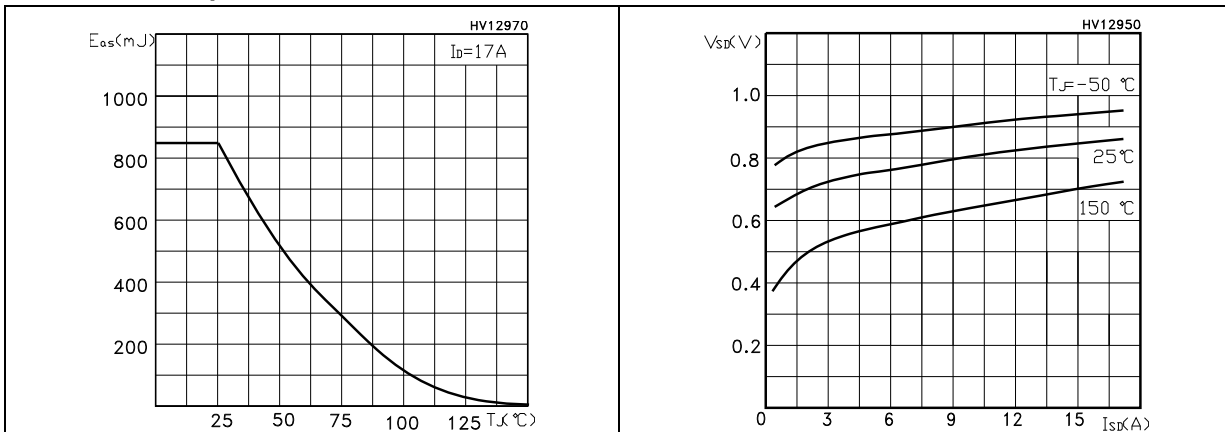


Figure 12. Maximum avalanche energy vs temperature Figure 13. Source-drain diode forward characteristic



### 3 Test circuits

**Figure 14. Switching times test circuit for resistive load**



AM01468v1

**Figure 15. Gate charge test circuit**



AM01469v1

**Figure 16. Test circuit for inductive load switching and diode recovery times**



AM01470v1

**Figure 17. Unclamped inductive load test circuit**



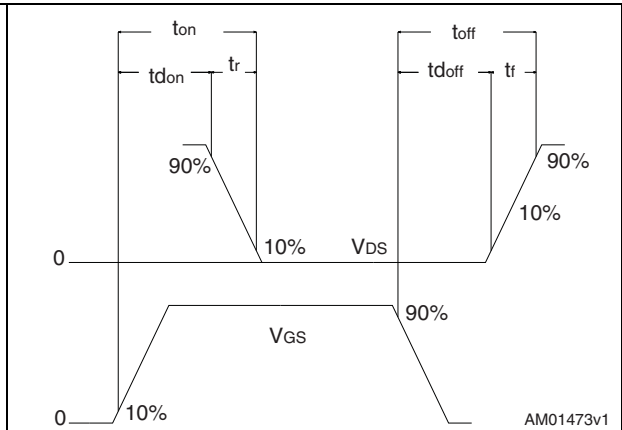
AM01471v1

**Figure 18. Unclamped inductive waveform**



AM01472v1

**Figure 19. Switching time waveform**



AM01473v1



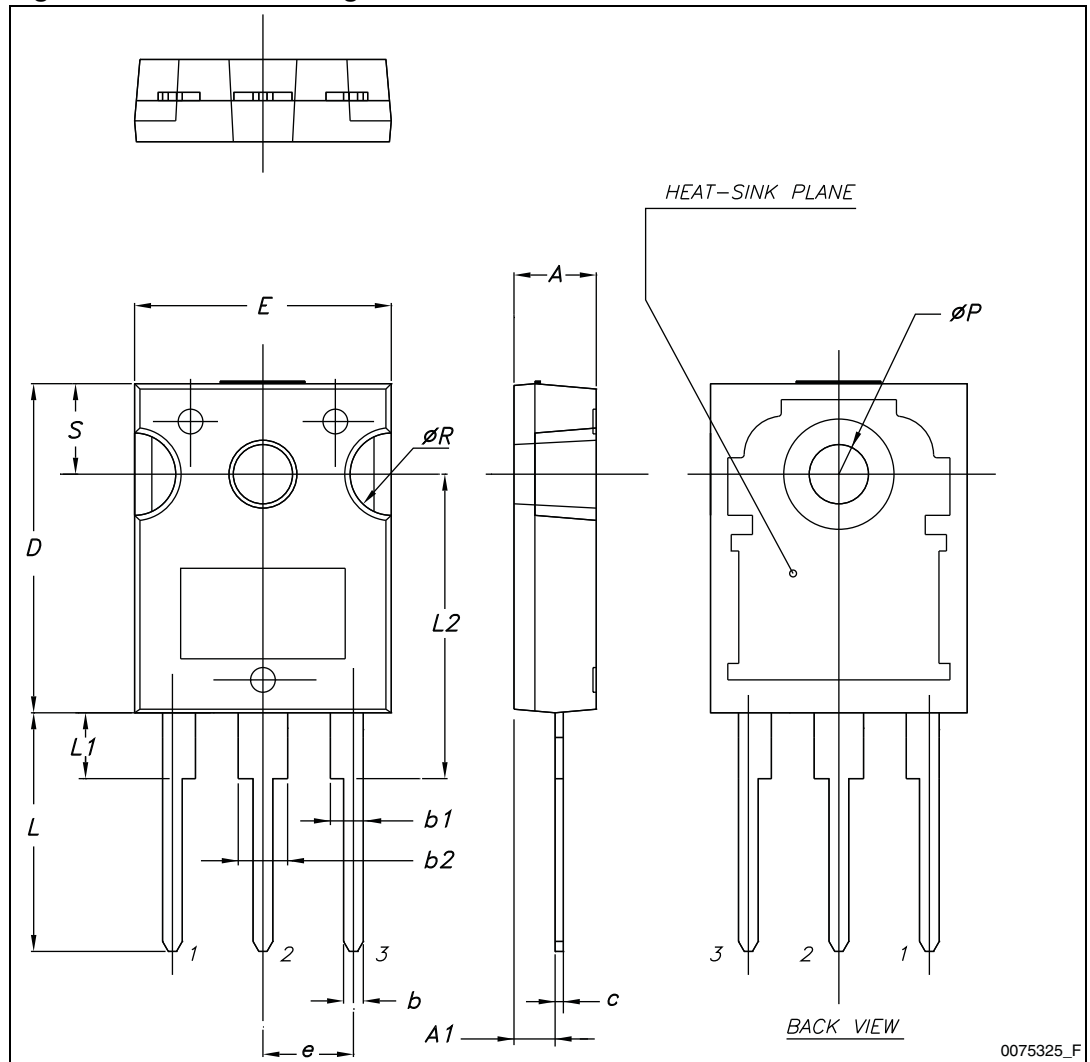
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

**Table 9. TO-247 mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S		5.50	

Figure 20. TO-247 drawing



0075325\_F

## 5 Revision history

Table 10. Document revision history

Date	Revision	Changes
05-Apr-2012	1	First release.

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